T.O. 31R2-2URC-81

TECHNICAL MANUAL

RADIO RECEIVER-TRANSMITTER, RT-1446/URC, P/N 10085-0000

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SAFETY SUMMARY

The following are general safety precautions that are not related to any specific procedures and therefore do not appear elsewhere in this publication. These are recommended precautions that personnel must understand and apply during many phases of operation and maintenance.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must at all times observe all safety regulations. Do not replace components inside the equipment with the power supply turned on. Under certain conditions, dangerous potentials may exist when the power control is in the off position, due to charges retained by capacitors. To avoid casualties, always remove power and discharge circuits to ground before touching any circuit components. Remove watches and rings before performing any maintenance procedures.

DO NOT SERVICE OR ADJUST ALONE

Under no circumstances should any person reach into or enter the enclosure for the purpose of servicing or adjusting the equipment except in the presence of someone who is capable of rendering aid.

RESUSCITATION

Personnel working with or near high voltages should be familiar with modern methods of resuscitation. Cardiopulmonary resuscitation procedures are outlined in T.O. 31-1-141-1, and annual refresher training requirements are outlined in AFOSH STD 127-50.

The following warnings appear in the text in this volume, and are repeated here for emphasis.

WARNING

Avoid breathing fumes generated by soldering. Eye protection is required.

WARNING

Dangerous voltages exist in this radio equipment. Before removing any cover, disconnect primary power.

WARNING

Do not dispose of lithium batteries in the trash. These batteries contain hazardous materials that can contaminate the environment.

HANDLING OF ELECTROSTATIC DISCHARGE SENSITIVE DEVICES (ESDS)

Electrostatic Discharge Sensitive Devices (ESDS) must be handled with certain precautions that must be followed to minimize the effect of static build-up. Consult T.O. 00-25-234, DOD Std-1686, and DOD HDBK 263. ESDS devices are identified in this technical order by the following symbol:

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GLOSSARY

A	Ampere(s)
A/D	Analog-to-Digital (Converter)
AFSK	Audio frequency shift keying; a baseband modulation scheme in which two audio frequencies are used to represent binary coded data; the frequency is shifted to one frequency to represent a 1 (mark) and to the other to represent a 0 (space).
AGC	Automatic gain control
ALE	Address latch enable
AM	Amplitude modulation; a modulation scheme in which the carrier is made to vary in amplitude in accordance with the modulating signal.
AME	Amplitude modulation equivalent
ANTIVOX	Prevents false VOX operation; see VOX
BFO	Beat Frequency Oscillator, used in SSB detection circuits
BIT	Built-in Test
BIU	Bus interface unit
BW	Bandwidth
CPU	Central processing unit
CREV	Converter reverse
CW	Continuous wave; a wave that does not vary in amplitude or frequency and is turned on and off to carry intelligence, e.g., Morse Code
D/A	Digital-to-Analog (Converter)
dB	Decibel(s)
dBm	Decibel(s) relative to one milliwatt
EMI	Electromagnetic interference
EPROM	Erasable programmable read-only memory
EU	Execution unit
HF	High frequency; a radio frequency band extending from about 3 MHz to 30 MHz; in this manual, HF includes 1.6 to 30 MHz.
HV	High voltage
IF	Intermediate frequency
IM	Intermodulation (distortion)
I/O	Input/Output
KREV	Keyer reverse
LCD	Liquid crystal display
LED	Light emitting diode
LPA	Linear power amplifier
LSB	Lower sideband; a modulation scheme in which the intelligence is carried on the first sideband below the carrier frequency; see SSB
MIC	Microphone
mA	Milliampere(s)
mV	Millivolt(s)
NBSV	Narrow band secure voice
PEP	Peak envelope power
PPC	Peak power control
PWB	Printed wiring board
RAM	Random access memory
rms	Root mean square
RTC	Real time clock
RX	Receive

GLOSSARY (Continued)

S TONE	Sidetone
SSB	Single sideband; a modulation scheme in which the intelligence is carried by one of the carrier sidebands, the other sideband and the carrier center frequency being suppressed
TGC	Transmitter gain control
TX	Transmit
uA	Microampere(s)
uP	Microprocessor
USB	Upper sideband; a modulation scheme in which the intelligence is carried on the first sideband above the carrier frequency; see SSB
uV	Microvolt(s)
Vac	Volts, alternating current
VCO	Voltage controlled oscillator
Vdc	Volts, direct current
VOX	Voice operated transmission
VSWR	Voltage standing wave ratio; the ratio of the maximum to the minimum voltage of a standing wave on a radio frequency transmission line
W	Watt(s)

INTRODUCTION

The purpose of this on-equipment level manual is to provide all information necessary for the installation, operation and on-equipment maintenance of Receiver-Transmitter, Radio, RT-1446/URC, manufactured by the RF Communications Group of Harris Corporation, Rochester, New York. The manual is divided into eight chapters. The contents of each chapter are briefly described in the following paragraphs.

Chapter 1 provides a general description and a list of capabilities and limitations of the Receiver-Transmitter, Radio, RT-1446/URC. A list of companion equipment references are included along with the components that form the RT-1446/URC.

Chapter 2 provides the information necessary for planning and carrying out the installation of the Receiver-Transmitter, Radio, RT-1446/URC. A dimensional outline drawing is provided to show dimensions and other information required for proper installation.

Chapter 3 provides instructions for preparing the Receiver-Transmitter, Radio, RT-1446/URC for use, including the initial application of power and checkout. Instructions for repacking the equipment for reshipment are also included in Chapter 3.

Chapter 4 provides complete operating instructions for the Receiver-Transmitter, Radio, RT-1446/URC in all modes and contains a list of operating controls and indicators.

Chapter 5 provides a complete theory of operation for the Receiver-Transmitter, Radio, RT-1446/URC. An overall theory and detailed theory of individual functional circuits are provided.

Chapter 6 describes the on-equipment location maintenance procedures. On-equipment location maintenance is based on the use of built-in test (BIT) features of the equipment to isolate problems to the replaceable subassembly or printed wiring board (PWB) level. Depot maintenance is supplied in a separate publication, T.O. 35C1-2-892-3. The Depot Manual is based on performance testing and trouble analysis of the subassembly or PWB to locate and replace faulty parts at the lowest replaceable unit level (LRU).

Chapter 7 contains the illustrated Parts Breakdown (IPB) information at the on-equipment level. This includes assemblies and parts that may be replaced at the on-equipment location.

Chapter 8 contains all fold-out (FO) drawings. A cross reference list is provided as well as the individual drawings referenced throughout chapters 1 to 7. The diagrams are numbered FO-1, FO-2, etc. They are printed on sheets with page-size blank aprons to permit viewing the diagram with the rest of the book closed or opened to another page.

APPLICABLE SPECIFICATIONS

The following specifications, standards, and publications were used in the preparation of this manual.

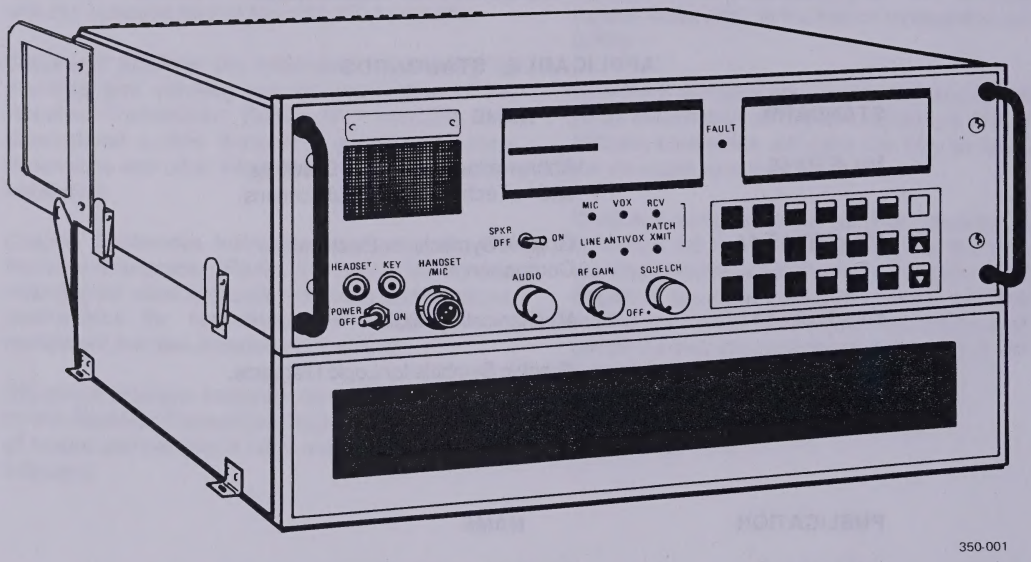
SPECIFICATION	NAME
MIL-M-38798B, para. 3.4	Combined Operation and Maintenance Instructions Manual (Equipment).
MIL-M-38807, Amend. 4	Preparation of Illustrated Parts Breakdown.
MIL-M-38790 and MIL-M-38784A	General Requirements for Preparation of Technical Manuals.

APPLICABLE STANDARDS

STANDARD	NAME
MIL-STD-12	Abbreviations for use on Drawings and in Technical Type Publications.
MIL-STD-15-1A	Graphic Symbols for Electrical Components.
MIL-STD-17-1	Mechanical Symbols.
MIL-STD-806	Graphic Symbols for Logic Diagrams.

APPLICABLE PUBLICATIONS

PUBLICATION	NAME
DOD 5200.20	Distribution Statements on Technical Documents.
USAS Y14.15-1966	Electrical and Electronic Diagrams.
USAS Y32.16-1968	Electrical and Electronic Reference Designations.
T.O. 31-1-141 (Series)	Technical Manual-Basic Electronic Technology and Testing Practices.



350-001

Figure 1-1. Radio Receiver-Transmitter RT-1446/URC

CHAPTER 1

GENERAL INFORMATION

1-1. GENERAL DESCRIPTION AND USE. Radio Receiver-Transmitter RT-1446/URC, shown in figure 1-1, is an all solid state, synthesized, single sideband (SSB) transceiver that operates in the high frequency (HF) band from 1.6 to 30 MHz, tunable in steps of 10 Hz. The RF output power of the transmitter section is 100 watts. The equipment is referred to as the 100 Watt Transceiver in the remainder of this manual. The 100 Watt Transceiver operates from a +13.6 Vdc power source. A Power Supply companion equipment PP-8092/URC is available when the 100 Watt Transceiver is to operate from 115/230 Vac and +12/28 Vdc sources.

a. Audio Inputs/Outputs. The 100 Watt Transceiver will accept keyline and audio inputs (voice or data) from a CW key, Handset/Mic, telephone line, narrow band secure voice (NBSV) equipment, or other source. A self-contained speaker and an externally connected headset provide for audible outputs of received voice and CW signals. Audio input/output connections are available at the 100 Watt Transceiver rear panel connectors.

b. Control Inputs. The 100 Watt Transceiver can be controlled locally using the front panel keypad to enter frequency, channel, and various mode selections. Analog controls set audio gain, RF gain, and squelch levels. The front panel LCD displays equipment operating parameters such as frequency and mode, plus Built-in Test (BIT) results. Up to 100 channels of operating frequency and mode information can be stored in memory. The keypad features, displays, and RF gain can be controlled via a remote control equipment (C-11329/URC, or equal). The remote interface is compatible with EIA Standards RS-232C and RS-422 as well as conventional telephone lines via an internal modem.

c. Built-In Test (BIT) Feature. The 100 Watt Transceiver built-in test (BIT) capability locates malfunctions to replaceable assemblies and subassemblies. BIT testing is initiated from the front panel keypad, or via a remote control equipment.

d. Power Requirements. The 100 Watt Transceiver power supply operates from 115 Vac, 230 Vac, 12 Vdc, or 28 Vdc voltage sources. The power supply is protected against overloads, electromagnetic interference, and reverse DC polarity.

1-2. EQUIPMENT FUNCTIONAL DESCRIPTION. A simplified block diagram of the 100 Watt Transceiver is shown in figure 1-2. The 100 Watt Transceiver can be used as a receiver-transmitter connected directly to an antenna or as an exciter to provide a 100 watt input to a separate Linear Power Amplifier (LPA).

a. Transmitter. In the transmit mode, the 100 Watt Transceiver accepts audio/keyline inputs from a CW key, handset/mic, telephone line, or other source, and impresses the audio on a 455 KHz Intermediate Frequency (IF) carrier. The 455 KHz IF is raised in two conversions to the 1.6 to 30 MHz transmitting range, and power amplified to a signal level of 100 watts Peak Envelope Power (PEP) or Average (AVG) into a 50 ohm load. A directional bridge in the transmit path measures the forward and reflected power levels. This information is used for front panel display and for transmitter gain control functions. A transmit-receive (T/R) switch separates the transmit and receive paths allowing connection to a common antenna.

b. Receiver. In the receive mode, the 1.6 to 30 MHz received signals bypass the power amplifier and are reduced to a 455 KHz IF using a double-conversion process. The first conversion is made at an IF of 40.455 MHz and band pass filtered to remove undesired image frequencies. The second conversion is made at an IF of 455 KHz and band pass filtered to achieve selectivity. The resulting 455 KHz IF signal is demodulated with an amplitude detector (AM mode) or product detector (SSB modes) to obtain the audio output.

c. Control. Control of the 100 Watt Transceiver is from the front panel or by remote input. Logic signals are processed by a microprocessor which provides the necessary memory, control, logic and timing to coordinate the functions of the 100 Watt Transceiver in all modes of operation. The microprocessor also controls the detection and display indications of the BIT circuits.

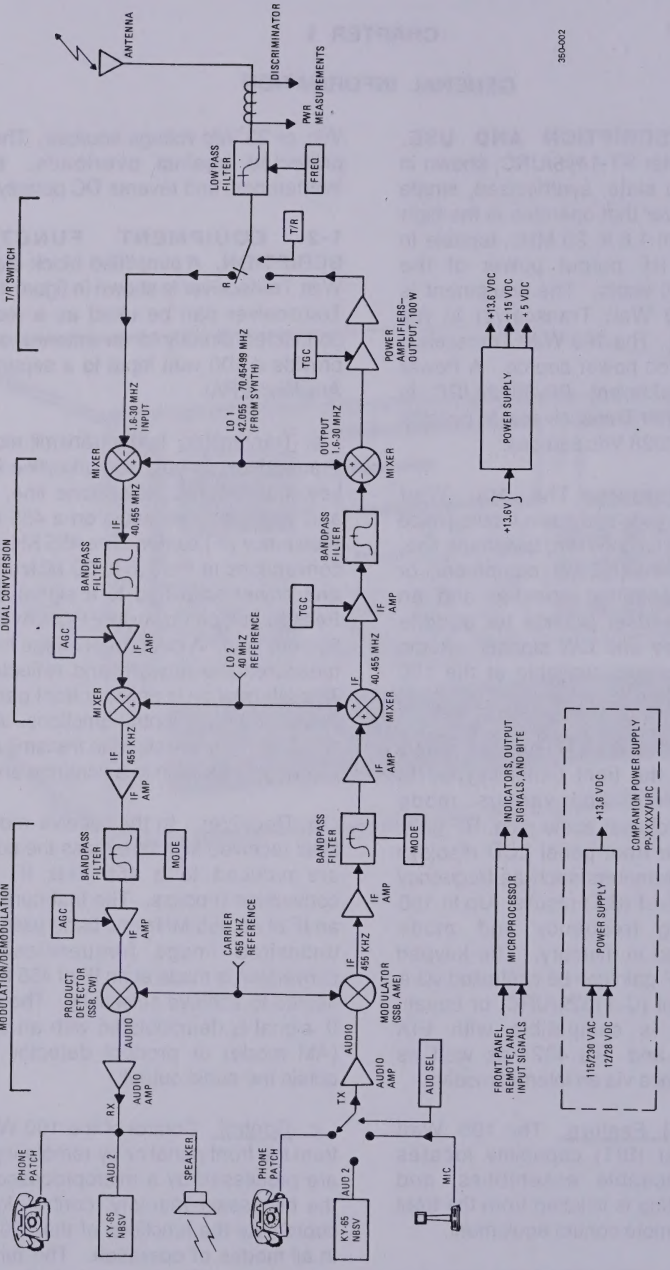


Figure 1-2. Simplified Functional Diagram, 100 Watt Transceiver

d. Reference Frequencies. The frequencies used in the modulation, demodulation, and double conversion processes are generated by the Synthesizer and Reference/BFO modules. All reference frequencies are derived from a stable 10 MHz standard frequency.

e. Power. Operating voltage is supplied from the power supply that operates from a selectable input voltage of 115 Vac, 230 Vac, 12 Vdc or 28 Vdc (nominal). The power supply has a single output of +13.6 Vdc which the multivoltage converter supply uses to generate output voltages of +5 Vdc and ±15 Vdc.

1-3. MECHANICAL DESIGN. The mechanical construction of the 100 Watt Transceiver is shown in figure 1-3.

a. Assembly Locations and Cooling Air Flow. The 100 Watt Transceiver contains all assemblies that perform transmitting and receiving functions, and operates from a +12 Vdc power source. A companion Power Supply equipment, PP-8092/URC, may be used when the 100 Watt Transceiver is to operate from a 115/230 Vac power source. The power supply has an output voltage of +13.6 Vdc, nominal, and is positioned as the lower unit when operated with the 100 Watt Transceiver. Cooling air is forced through the Power Supply by a fan that draws air in through a filter on the front of the Power Supply, over heat sink fins on the Power Supply, and finally forces it out and upward at the rear of the unit over the 100 Watt Transceiver fins on the power amplifier assembly. The cooling fan has two speeds. When the equipment is operating at normal or low temperature, the fan runs at low speed. When the equipment temperature has increased to a level that requires additional cooling, the fan runs at high speed. An automatic temperature sensing system determines the correct fan speed.

b. Assembly Accessibility. The 100 Watt Transceiver typically is operated with the Power Supply assembly. The two main assemblies are hinged at the rear, and the Power Supply can have drawer slides attached so that the 100 Watt Transceiver can be rack-mounted. The 100 Watt Transceiver, when operated with the companion Power Supply, can then be unlatched, raised and supported by a rod in a tilted position without removing the 100 Watt Transceiver from the rack (figure 1-3, sheet 4). In this position, the +13.6 Vdc power supply and the two assemblies on the underside of the 100 Watt Transceiver assembly are accessible for removal or maintenance. When the 100 Watt Transceiver cover is removed, a tray assembly, which is hinged at the rear, can be raised and locked in position to make assemblies accessible within the 100 Watt Transceiver assembly. The front panel assembly can be pulled forward and tilted downward to make attached assemblies accessible for maintenance or removal.

1-4. LEADING PARTICULARS. General characteristics of the 100 Watt Transceiver are summarized in Table 1-1, Leading Particulars. This table includes all physical data and operating/storage environment data. Functional characteristics of the equipment are discussed in paragraph 1-23 and listed in table 1-2 in this manual.

1-5. CAPABILITIES AND LIMITATIONS. The functional and operational characteristics of the 100 Watt Transceiver are described in Table 1-2, Capabilities and Limitations.

1-6. EQUIPMENT AND ACCESSORIES SUPPLIED. Table 1-3 lists all of the supplied assemblies, components, units, cables, and accessory kits that pertain to the 100 Watt Transceiver.

1-7. EQUIPMENT REQUIRED BUT NOT SUPPLIED.

a. Antenna System. An antenna is required (not supplied) for operation of the 100 Watt Transceiver. Since the 100 Watt Transceiver operates in the transceive mode, a single antenna is used for both receiving and transmitting signals. The required characteristic load impedance of the antenna is 50 ohms, unbalanced, at the 100 Watt Transceiver frequency of operation. If the antenna does not exhibit a constant 50 ohm impedance over the frequency range of operation, an accessory antenna coupler (CU-2310/URC) is required. The antenna coupler effects an impedance match between the 100 Watt Transceiver and the antenna, such that the 100 Watt Transceiver always has a constant 50 ohm load.

b. Ancillary Equipment. The combination of the 100 Watt Transceiver equipment and an antenna system will allow voice and CW operation without further additional equipment or supplies. However, in the typical 100 Watt Transceiver installation, the 100 Watt Transceiver interfaces with various ancillary

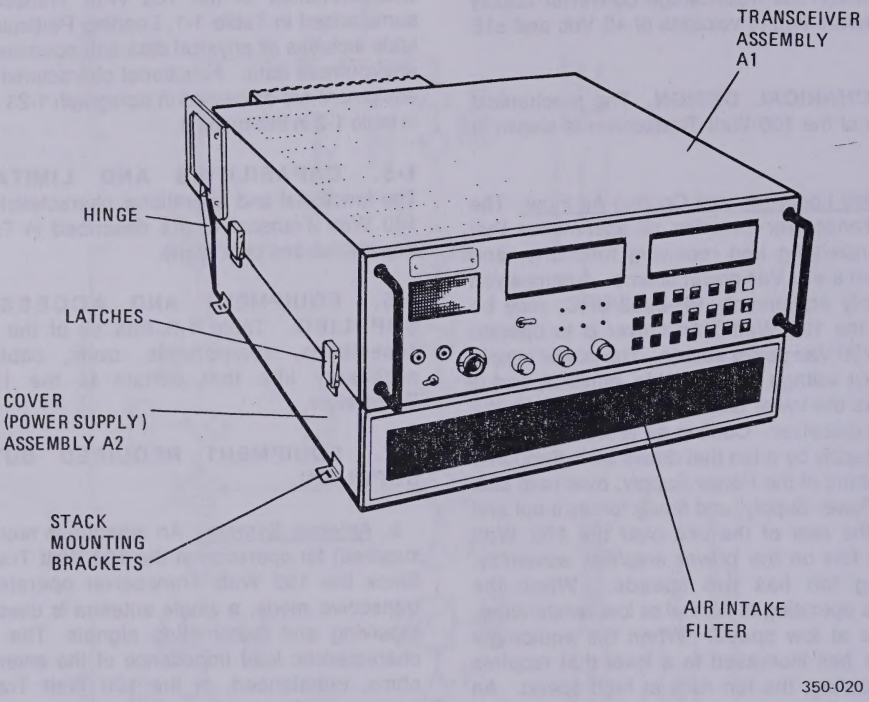


Figure 1-3. Identification of Subassemblies, 100 Watt Transceiver (Sheet 1 of 4)

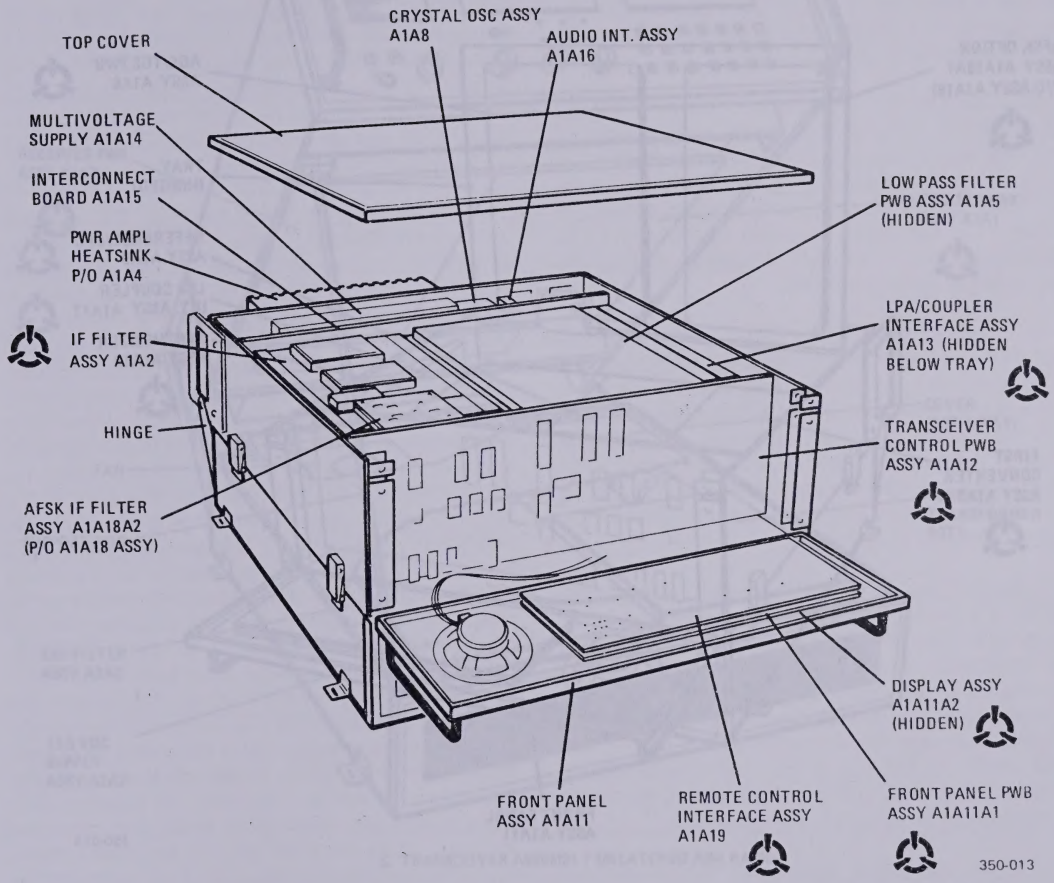

TOP COVER
CRYSTAL OSC ASSY A1A8
AUDIO INT. ASSY A1A16
MULTIVOLTAGE SUPPLY A1A14
INTERCONNECT BOARD A1A15
PWR AMPL HEATSINK P/O A1A4
LOW PASS FILTER PWB ASSY A1A5 (HIDDEN)
IF FILTER ASSY A1A2
LPA/COUPLER INTERFACE ASSY A1A13 (HIDDEN BELOW TRAY)
HINGE
TRANSCEIVER CONTROL PWB ASSY A1A12
AFSK IF FILTER ASSY A1A18A2 (P/O A1A18 ASSY)
DISPLAY ASSY A1A11A2 (HIDDEN)
FRONT PANEL ASSY A1A11
REMOTE CONTROL INTERFACE ASSY A1A19
FRONT PANEL PWB ASSY A1A11A1
350-013

Figure 1-3. Identification of Subassemblies, 100 Watt Transceiver (Sheet 2 of 4)

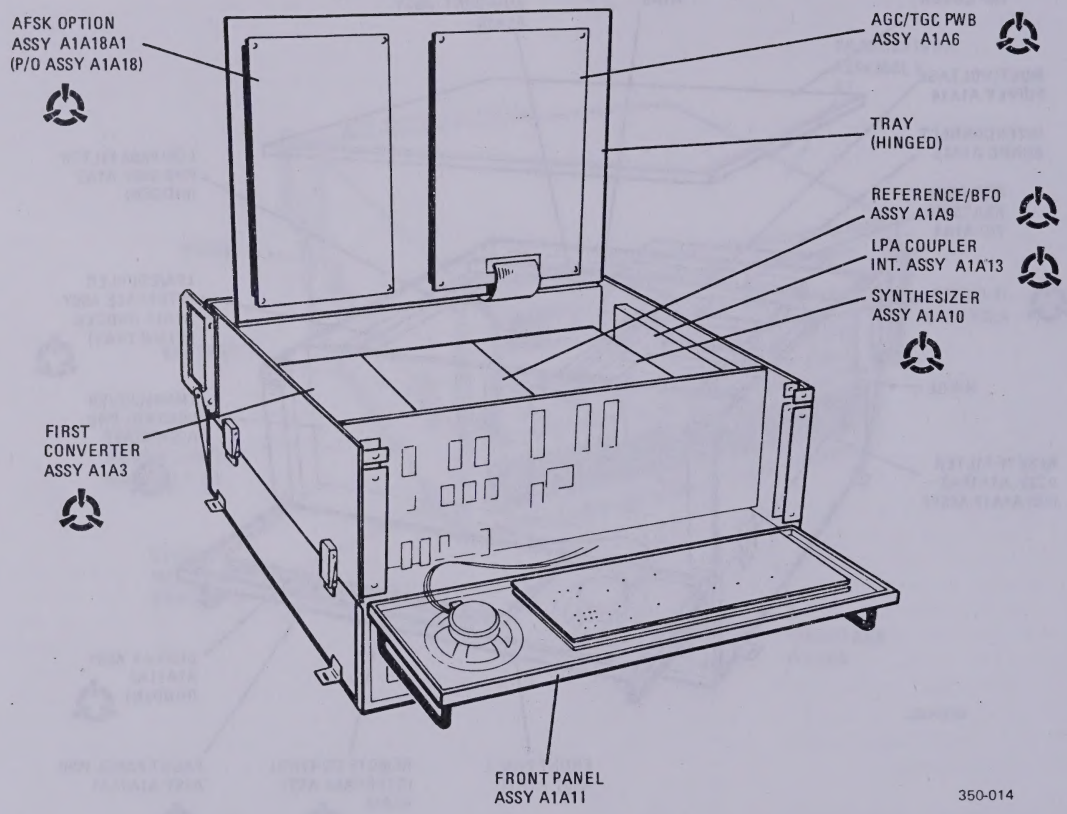


Figure 1-3. Identification of Subassemblies, 100 Watt Transceiver (Sheet 3 of 4)

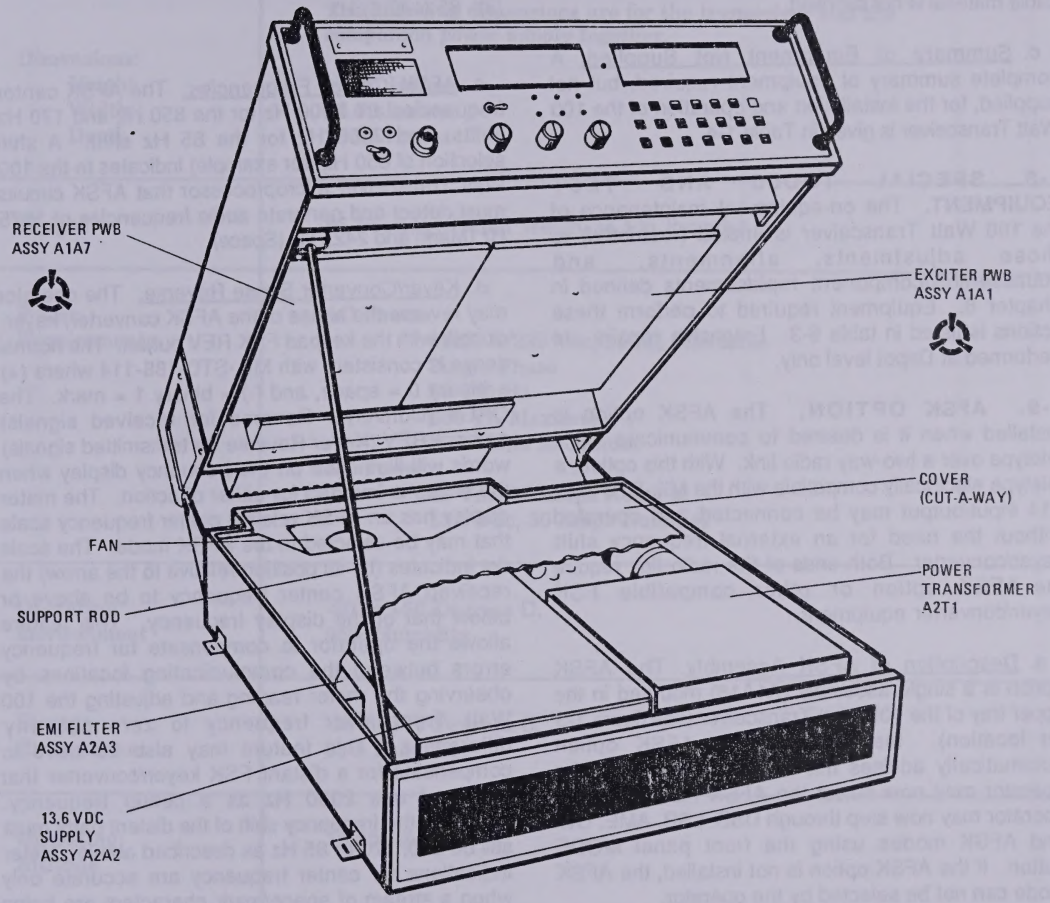


Figure 1-3. Identification of Subassemblies,100 Watt Transceiver (Sheet 4 of 4)

equipment such as modems, telephone lines, remote audio sources, remote control lines, and various keylines. In these applications it will be necessary to fabricate cables for interconnection. Certain connectors for interconnections are supplied in the 100 Watt Transceiver ancillary kit, but the required cable material is not supplied.

c. Summary of Equipment Not Supplied. A complete summary of equipment required, but not supplied, for the installation and operation of the 100 Watt Transceiver is given in Table 1-4.

1-8. SPECIAL TOOLS AND TEST EQUIPMENT. The on-equipment maintenance of the 100 Watt Transceiver is limited (restricted) to those adjustments, alignments, and subassembly/component replacements defined in chapter 6. Equipment required to perform these actions is listed in table 6-3. Extensive repairs are performed at Depot level only.

1-9. AFSK OPTION. The AFSK option is installed when it is desired to communicate via a teletype over a two-way radio link. With this option, a teletype electrically compatible with the MIL-STD-188-114 input/output may be connected and operated without the need for an external frequency shift keyer/converter. Both ends of the radio link require the AFSK option or other compatible FSK keyer/converter equipment.

a. Description of AFSK Assembly. The AFSK option is a single assembly (A1A18) mounted in the upper tray of the 100 Watt Transceiver (see figure 1-3 for location). Installation of the AFSK option automatically advises the microprocessor that the operator may now select the AFSK mode, i.e., the operator may now step through USB, LSB, AME, CW and AFSK modes using the front panel MODE button. If the AFSK option is not installed, the AFSK mode can not be selected by the operator.

b. AFSK Sideband Selection. Shift/sideband select switches are located on the AFSK assembly (filter portion). When the AFSK option is installed, the switches must be placed into one of six combinations:

S1 - Shift	S2 - AFSK Sideband
(1) 850 (±425) Hz	(1) Lower Sideband (LSB)
(2) 170 (±85) Hz	(2) Upper Sideband (USB)
(3) 85 (±42.5) Hz	

c. AFSK Center Frequencies. The AFSK center frequencies are 2000 Hz for the 850 Hz and 170 Hz shifts, and 2805 Hz for the 85 Hz shift. A shift selection of 850 Hz (for example) indicates to the 100 Watt Transceiver microprocessor that AFSK circuits must detect and generate audio frequencies of 1575 Hz (Mark) and 2425 Hz (Space).

d. Keyer/Converter Sense Reverse. The operator may reverse the sense of the AFSK converter, keyer, or both with the keypad FSK REV button. The normal sense is consistent with MIL-STD-188-114 where (+) = binary 0 = space, and (-) = binary 1 = mark. The CREV (Converter Reverse for received signals) and/or KREV (Keyer Reverse for transmitted signals) words will illuminate on the frequency display when the sense is inverted for either direction. The meter display has an AFSK relative center frequency scale that may be selected in the AFSK mode. The scale dot indicates (by its position relative to the arrow) the received AFSK center frequency to be above or below that of the display frequency. This feature allows the operator to compensate for frequency errors between the communicating locations by observing the meter reading and adjusting the 100 Watt Transceiver frequency to zero out any differences. This feature may also be used to compensate for a distant FSK keyer/converter that does not use 2000 Hz as a center frequency. However, the frequency shift of the distant party must still be 850, 170 or 85 Hz as described above. Meter indications for center frequency are accurate only when a stream of space/mark characters are being received. Care must be taken to avoid off-channel operation when the frequency is adjusted to compensate for the distant station, as this changes the transmit frequency.

1-10. RELATED PUBLICATIONS. The 100 Watt Transceiver is described in this manual and in the other related publications listed in table 1-6. Table 1-6 also lists related publications that may apply to accessory equipment listed in table 1-5.

Table 1-1. Leading Particulars

Item	Characteristic or Value
Dimensions: Height Width Depth	**NOTE** The following dimensions are for the transceiver and the companion power supply together. 8.75 Inches 16.75 Inches 20.00 Inches
Weight	85 Pounds (Crated Weight is 105 Pounds)
Power Requirements	AC Power 115/208/230 Vac, ±10%, selectable Single Phase 50-400 Hz 600 VA Maximum 500 Watts Maximum DC Power 28 Vdc, 15 Amps Nominal 13.6 Vdc, 30 Amps Nominal
Operating Environment	-30 to +50 Degrees C. 95% Humidity
Storage Environment	-35 to +70 Degrees C. 95% Humidity
Operating Altitude	10,000 Feet
Transport Altitude	40,000 Feet
Shock/Vibration	MIL-STD-810C
Cooling	Convection, natural and forced air (built-in fan)

Table 1-1. Leading Particulars (Continued)

Item	Characteristic or Value
Cabling Requirements (Note: Only J1 connection is required for simple operation of the 100 Watt Transceiver with J2-J9 for extended use, and J6 mates with P8 from the Power Supply.	Rear Panel Connections-100 Watt Transceiver J1 - RF Input/Output J2 - RF Sample J3 - AFSK Interface J4 - Audio 2 (AUD2) J5 - Antenna Coupler J6 - Power J7 - Aux Power Out J8 - Linear Power Amplifier (LPA) J9 - Remote Control Interface TB1- Audio Interface Rear Panel Connections-Power Supply J1 - Primary Power Input P8 - Power Output
Transportability	Manual Methods Apply
Set-up Time	Less than 1 hour

Table 1-2. Capabilities and Limitations

Description of Characteristic	
Frequency Range:	1.600,00 MHz to 29.999,99 MHz
Frequency Tuning Resolution:	10 Hz Increments
Tuning:	Continuous and automatic
Frequency Accuracy:	Within 10 Hz of displayed operating frequency

Table 1-2. Capabilities and Limitations (Continued)

Description of Characteristic	
Channel Memory:	100-channel capacity; capable of being loaded locally or remotely with frequency and mode of operation. Retention of operational parameters without primary power is provided indefinitely with internal lithium battery.
Readout/Display	FREQUENCY, CHANNEL, BFO, MODE, AGC, LPA, VOX, AUDIO, POWER, VSWR, AFSK, BIT, SIGNAL STRENGTH
BFO	Variable ± 1 KHz, selectable in 10 Hz steps
Modes of Operation:	USB, LSB, AME, CW, AFSK (optional).
Sensitivity:	SSB: 0.5 uv for 10 dB S+N/N AM: 3 uv for 10 dB S+N/N
AGC Characteristics:	Attack Time: SSB 30 msec. max. Release Time: Front panel selectable; SLOW - 3 ± 1 second. MEDIUM - 200 ± 100 milliseconds. FAST - 30 milliseconds or less.
Audio Output:	4 watts to internal speaker
Selectivity:	SSB: nominally 350-3050 Hz at 3 dB.
Image and IF Rejection	Greater than 80 dB
Overload Protection	Receiver protected for input to 100 Vrms
FSK Modem Interface	MIL-STD-188-114 (low level)

Table 1-2. Capabilities and Limitations (Continued)

Description of Characteristic	
FSK Center Frequency and Shift	2805 ± 42.5 Hz 2000 ± 85 Hz 2000 ± 425 Hz
BIT	Fault isolation to replaceable module level, with front panel test initiation and alphanumeric indication of faults
Remote Control	Microprocessor based system capable of accepting data in accordance with any one of the following formats: EIA Std RS-232-C EIA Std RS-422 May also be operated over standard telephone links via an internal modem.
Remote Control Functions:	All 100 Watt Transceiver front panel functions, including Frequency, Channel Select, Mode, AGC, BFO, Fault-BIT Status, RF Gain, and Channel Load
Power Output	SSB, 100 PEP/Average; compatible AM, 25 watt carrier nominal, CW 100 watt PEP
Overload Protection	Power amplifier is fully protected from mismatch, including an open or shorted antenna.
Carrier Suppression (A3J Mode)	At least 50 dB below PEP output
Intermodulation Distortion	33 dB below PEP
Undesired Sideband Suppression	50 dB at 1 kHz

Table 1-2. Capabilities and Limitations (Continued)

Description of Characteristic	
Harmonic Suppression	2nd 40 dB, 3rd 55 dBm 50-400 MHz 70 dB below PEP
Audio Input	Dynamic microphone; in addition, a 600 ohm input is provided
(Table 1-3. Equipment and Accessories Supplied, is deleted)	

Table 1-4. Equipment Required but not Supplied *

Qty	Item	Description
1	Ancillary Kit, 10085-0060. consisting of the items the items listed below.	Miscellaneous items that can be attached from the 100 Watt Transceiver for shipment.
1	Connector, Receptacle, 9 pin D-type, DEM 9S	Mates to J4 of the 100 Watt Transceiver

Table 1-4. Equipment Required but not Supplied* (Continued)

1	Power Cable Assembly, 10085-0065	Connects the 100 Watt Transceiver to the 115/208/230 Vac power source
1	CW Key, 10085-0066	Key for CW operation
1	Handset, 10085-0067	Voice operation
4	Bumper, Recessed, 827S	For table mounting
4	Stack Mount Brackets	For stacking the 100 Watt Transceiver on top of the LPA
1	Microphone, 10085-0068	Voice operation
1	Hood, D-commector, 9 position, DE24657	For connector DEM 9S
1	Screw Lock Assembly, D20419-16	Retaining screws for connector DEM 9S
1	Transmit/Receive Antennna	Connects to J1 at rear of 100 Watt Transceiver. Required for reception and transmission of radio signals. If antenna does not exhibit a 50 ohm impedance at the operating frequency, and antenna coupler is required. (See antenna couplers below.)
1 drop per screw	Loctite #242 (Blue)	For screws fastening handles to front panel (See Fig. 7-3).

*For test equipment required, refer to table 6-3.

Table 1-5. Optional Equipment

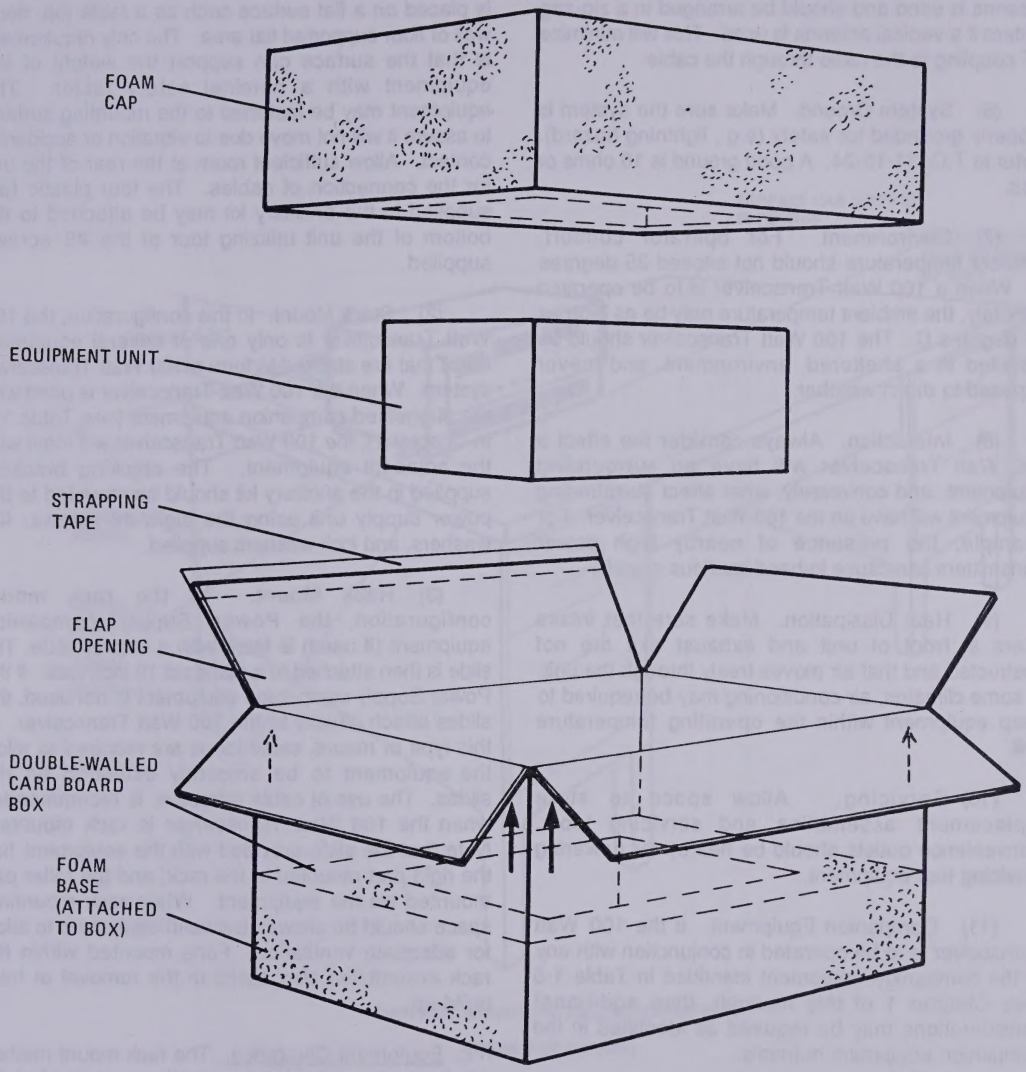
Qty	Item	Description
1	Antenna Coupler (100/500 watt) (RF-351) CU-2310/URC	Companion equipment to antenna as required. Connects between the 100 Watt Transceiver and antenna to effect an impedance match between the two. Power handling is 500 watts, PEP, 250 watts AVG maximum, and is compatible with the 100 Watt Transceiver.
1	Antenna Coupler (1000 watts) (RF-601A) AN/URA-38()	Companion equipment to item 1 as required. Connects between the 1 KW LPA and the antenna to effect an impedance match between the two. Power handling is 1000 watts PEP/AVG maximum, and is compatible with the 100 Watt Transceiver/ 1KW LPA configuration (see 1KW LPA below).
1	Radio Frequency Linear Power Amplifier (LPA) (500 watts) (RF-355) AM-7223/URC	Companion equipment used only when it is desired to increase the output transmission level of the 100 Watt Transceiver from 100 watts to 500 watts. Unit is compatible with the 100 Watt Transceiver, and the 100/500 Watt Antenna Coupler.
1	Radio Frequency LPA 28 Vdc Inverter (RF-367) PP-8093/URC	Companion equipment used only when it is desired to operate the 500W LPA from a 28 Vdc source.

Table 1-5. Optional Equipment (Continued)

Qty	Item	Description
1	Radio Frequency Amplifier (1000 watts) (RF-353) AM-7224/URC	Companion equipment used only when it is desired to increase the output transmission level of the 100 Watt Transceiver from 100 watts to 1000 watts. Unit is compatible with the 100 Watt Transceiver, and the 1000 watt antenna coupler.
1	Power Supply (RF-354) PP-7913/URC	Supplied with 1 KW LPA.
	Remote Control Unit (RF-352) C-11329/URC	Companion equipment used when it is desired to operate the 100 Watt Transceiver from a remote location.
	AFSK Option 10085-6000	Allows communication via teletype over a two-way radio link.
1	Transport Case CY-8358/URC	Allows convenient packing method for movement of equipment. Case is equipped with a DC power cable.
1	Power Cable, DC 10085-0064	For connecting to a DC primary power source.

Table 1-6. Related Publications

Title	Publication No.
100/500 Watt Antenna Coupler, CU-2310/URC	
On-Equipment Manual	TO 31RS-2URC-111
Depot Manual	TO 31R2-2URC-113
Work Cards	TO 31R2-2URC-116WC-1
Receiver-Transmitter, Radio, RT-1446/URC	
On-Equipment Manual	TO 31R2-2URC-81
Depot Manual	TO 31R2-2URC-83
Work Cards	TO 31R2-2URC-86WC-1
Amplifier, Radio Frequency, AM-7223/URC	
On-Equipment Manual	TO 31R2-2URC-101
Depot Manual	TO 31R2-2URC-103
Work Cards	TO 31R2-2URC-106WC-1
Power Supply, PP-7913/URC	
On-Equipment Manual	TO 35C1-2-892-1
Depot Manual	TO 35C1-2-892-3
Work Cards	TO 35C1-2-892-6WC-1
Amplifier, Radio Frequency, AM-7224/URC	
On-Equipment Manual	TO 31R2-2URC-121
Depot Manual	TO 31R2-2URC-123
Work Cards	TO 35C1-2-892-6WC-1
Remote Control Unit, C-11329/URC	
On-Equipment Manual	TO 31R2-2URC-91
Depot Manual	TO 31R2-2URC-93
Work Cards	TO 31R2-2URC-96WC-1
1KW Antenna Coupler Group, AN/URA-38A RF601 DR-525	TO 31R2-2URA38-1 TO 31R2-2TSC38-82 TO 31S1-4-228-1



UNPACKING PROCEDURE

1. PLACE BOX ON FLOOR WITH ARROWS MARKED ON EACH SIDE POINTING UP.
2. CUT TAPE ON TOP OF BOX AND REMOVE FOAM CAP FROM BOX.
3. LIFT EQUIPMENT UNIT OUT OF BOX.
4. SAVE BOX AND FOAM CAP FOR RESHIPMENT.

350-003

Figure 2-1. Unpacking the Equipment

be perpendicular to the elements if a horizontal antenna is used and should be arranged in a zig-zag pattern if a vertical antenna is used. This will minimize RF coupling to the radio through the cable.

(6) System Ground. Make sure the system is properly grounded for safety (e.g., lightning hazard). Refer to T.O. 31-10-24. A good ground is 10 ohms or less.

(7) Environment. For operator comfort, ambient temperature should not exceed 25 degrees C. When a 100 Watt Transceiver is to be operated remotely, the ambient temperature may be as high as 50 degrees C. The 100 Watt Transceiver should be installed in a sheltered environment and never exposed to direct weather.

(8) Interaction. Always consider the effect a 100 Watt Transceiver will have on surrounding equipment, and conversely, what effect surrounding equipment will have on the 100 Watt Transceiver. For example, the presence of nearby high power transmitters can cause in-band spurious signals.

(9) Heat Dissipation. Make sure that intake filters at front of unit and exhaust exit are not obstructed and that air moves freely through the unit. In some climates, air conditioning may be required to keep equipment within the operating temperature limit

(10) Servicing. Allow space to store replacement assemblies and servicing tools. Convenience outlets should be nearby for powering servicing test equipment.

(11) Companion Equipment. If the 100 Watt Transceiver is to be operated in conjunction with any of the companion equipment identified in Table 1-5 (see Chapter 1 of this manual), then additional considerations may be required as identified in the companion equipment manuals.

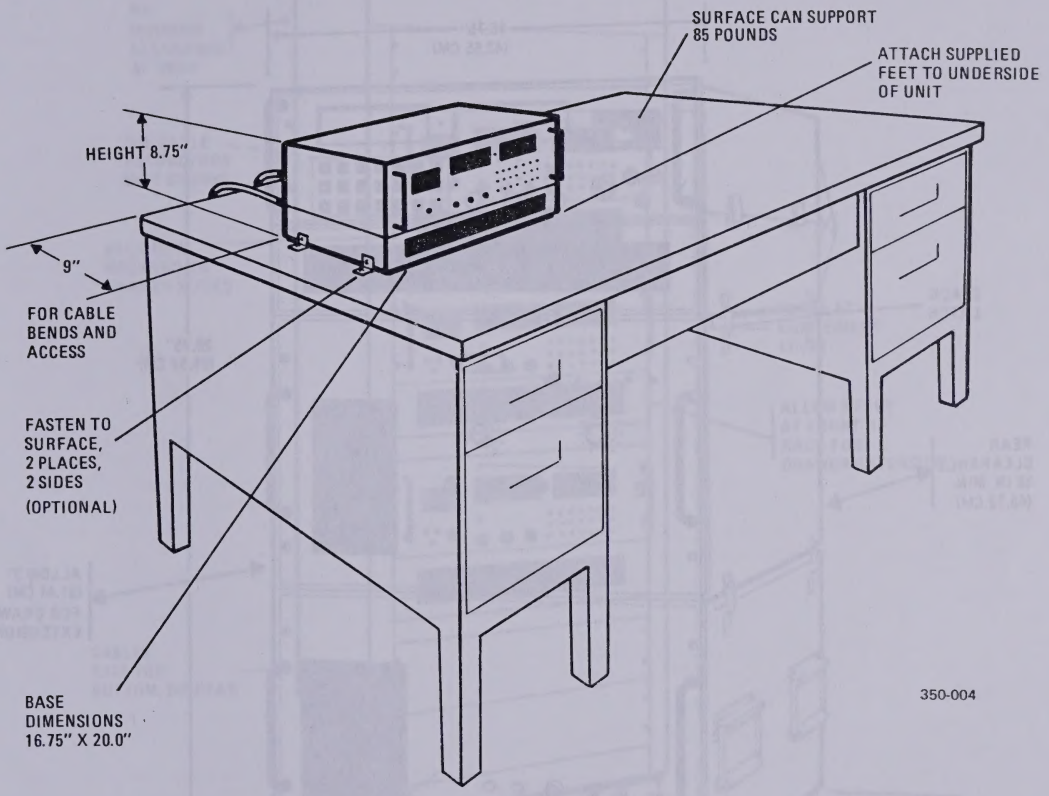
b. Equipment Mounting. Once the site has been selected, the method of mounting the equipment should be considered. Each mounting method requires a particular type of hardware. The mounting holes at the sides of the equipment can be used for slide mounts, brackets, latches, etc., depending on the manner of installation. Figure 2-2 illustrates the outline dimensions of the 100 watt transceiver, and figure 2-3 illustrates installations that typically result in one of the following mounting techniques.

(1) Surface Mount. The 100 Watt Transceiver is placed on a flat surface such as a table top, floor, wall or floor supported flat area. The only requirement is that the surface can support the weight of the equipment with a nominal safety factor. The equipment may be fastened to the mounting surface to assure it will not move due to vibration or accidental contact. Allow sufficient room at the rear of the unit for the connection of cables. The four plastic feet supplied in the ancillary kit may be attached to the bottom of the unit utilizing four of the #6 screws supplied.

(2) Stack Mount. In this configuration, the 100 Watt Transceiver is only one of several equipment items that are stacked to form a 100 Watt Transceiver system. When the 100 Watt Transceiver is used with the suggested companion equipment (see Table 1-4 in Chapter 1), the 100 Watt Transceiver will mate with the adjacent equipment. The stacking brackets supplied in the ancillary kit should be mounted to the power supply unit using the eight #6 screws, flat washers, and lock washers supplied.

(3) Rack Mount. In the rack mount configuration, the Power Supply companion equipment (if used) is fitted with a drawer slide. The slide is then attached to a standard 19 inch rack. If the Power Supply companion equipment is not used, the slides attach directly to the 100 Watt Transceiver. In this type of mount, cable loops are required to allow the equipment to be smoothly extended on the slides. The use of cable retractors is recommended when the 100 Watt Transceiver is rack mounted. Note that the slide provided with the equipment has the rigid part mounted in the rack, and the roller part mounted on the equipment. When rack mounting, space should be allowed between equipment to allow for adequate ventilation. Fans mounted within the rack assemblies also assist in the removal of heat build-up.

c. Equipment Clearance. The rack mount method eliminates the need for access clearance behind the equipment. A 19 inch rack may be positioned close to a wall and access to the rear of the unit gained via the extension of the 100 Watt Transceiver on slides. However, in such an installation, careful consideration must be given to cooling and venting of the unit. Upon completion of preparation for installation, continue to Section II, Installation Procedure.



SURFACE MOUNT INSTALLATION DETAIL

(DESK TOP SHOWN)

Figure 2-3. Installation Diagram (Sheet 1 of 3)

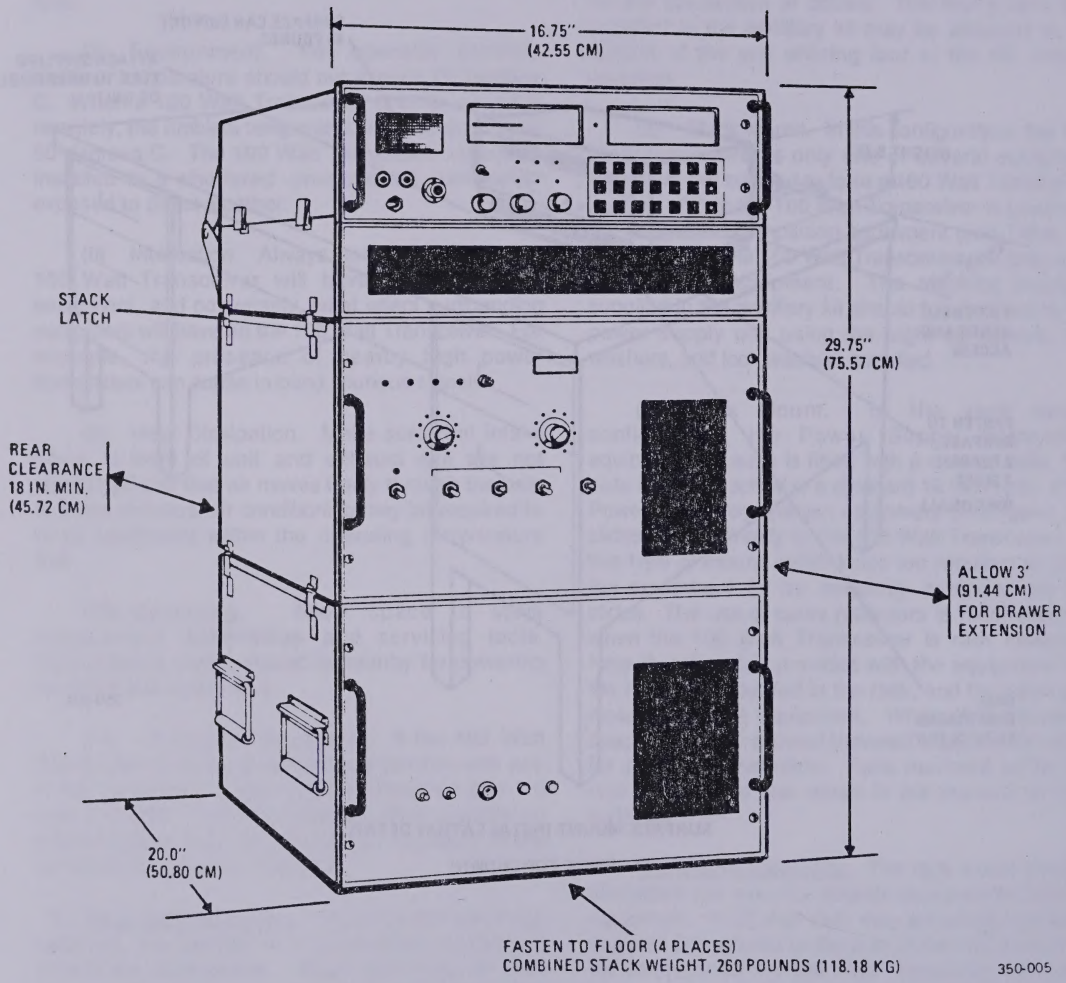
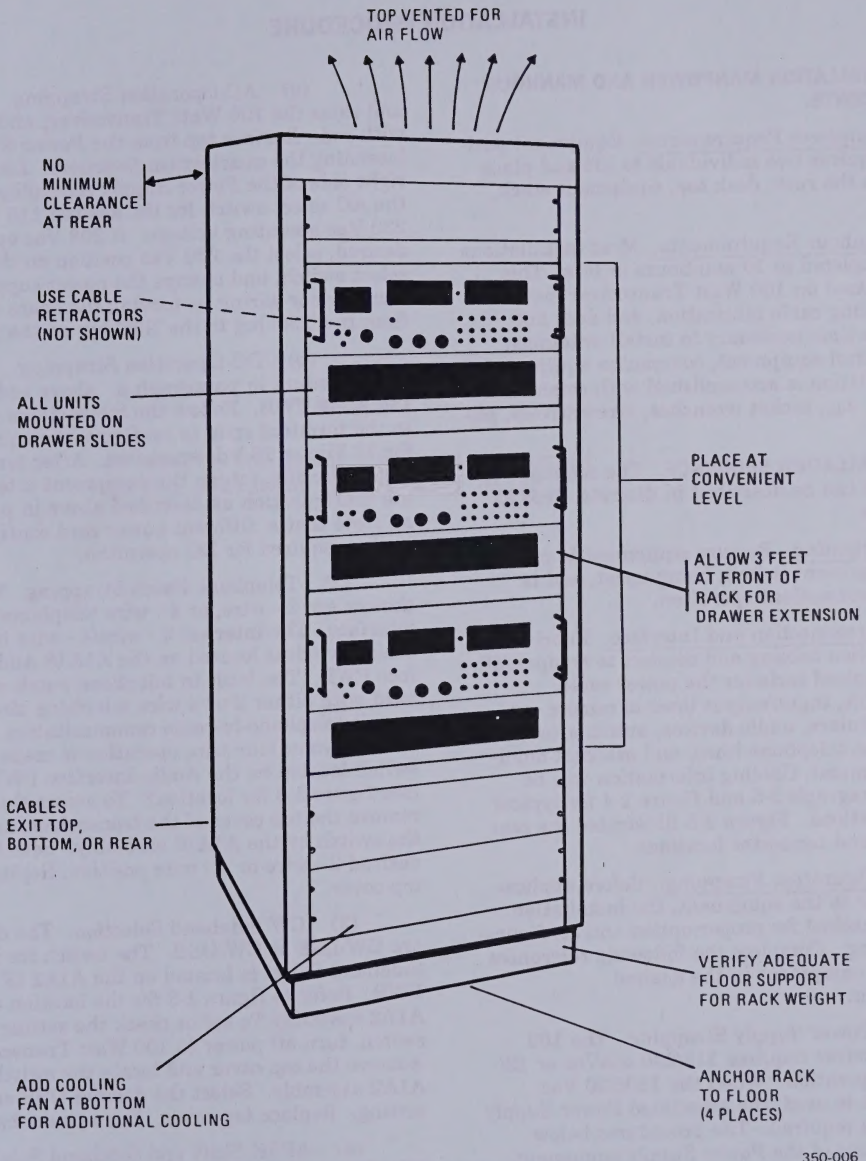


Figure 2-3. Installation Diagram (Sheet 2 of 3)


TOP VENTED FOR AIR FLOW
NO MINIMUM CLEARANCE AT REAR
USE CABLE RETRACTORS (NOT SHOWN)
ALL UNITS MOUNTED ON DRAWER SLIDES
PLACE AT CONVENIENT LEVEL
ALLOW 3 FEET AT FRONT OF RACK FOR DRAWER EXTENSION
CABLES EXIT TOP, BOTTOM, OR REAR
VERIFY ADEQUATE FLOOR SUPPORT FOR RACK WEIGHT
ANCHOR RACK TO FLOOR (4 PLACES)
ADD COOLING FAN AT BOTTOM FOR ADDITIONAL COOLING
350-006

RACK MOUNT INSTALLATION DETAIL.

(THREE UNITS, TYPICAL INSTALLATION SHOWN)

Figure 2-3. Installation Diagram (Sheet 3 of 3)

SECTION II

INSTALLATION PROCEDURE

2-3. INSTALLATION MANPOWER AND MANHOUR REQUIREMENTS.

a. Manpower Requirements. Equipment positioning requires two individuals to lift and place the unit in the rack, desk top, equipment stack, etc.

b. Manhour Requirements. Most installations can be completed in 10 manhours or less. This figure is based on 100 Watt Transceiver installation, including cable fabrication, and does not include the time necessary to install antennas, remote control equipment, companion equipment, etc. Installation is accomplished with common hand tools, e.g., socket wrenches, screwdrivers, pliers, etc.

2-4. INSTALLATION SEQUENCE. The sequence of installation can be described in discrete steps as listed below.

a. Positioning. Be sure equipment is properly secured to prevent it from being upset, and is located for convenient operation.

b. Interconnection and Interface. Fabricate interconnection cabling and connect to equipment. Cabling required includes the power cable, antenna cable, input/output lines to remote controls, teleprinters, audio devices, antenna coupler, microphones, telephone lines, and external monitoring equipment. Cabling information will be found in paragraph 2-5 and figure 2-4 for typical cable fabrications. Figure 2-5 illustrates the rear panel view and connector locations.

c. Configuration Strapping. Before application of power to the equipment, the installation should be checked for proper option and configuration strapping. Complete the following references to strap the equipment in the desired configuration:

(1) Power Supply Strapping. The 100 Watt Transceiver requires 115/230 46eVac or 12/28 Vdc for operation. When the 110/220 Vac power source is used, the associated Power Supply equipment is required. The procedures below assume the use of the Power Supply equipment. The power cord supplied is for ac operation only. If +13.6 V dc operation is desired, use DC Power Cable, Harris Part Number 10085-0064. To strap the 100 watt transceiver for the desired ac or dc voltage, use one of the procedures below.

(a) AC Operation Strapping. Unlatch and raise the 100 Watt Transceiver, and support with rod. Remove top from the Power Supply by loosening the quarterturn fasteners. Locate the right side of the Power Supply Assembly. Position the AC select switch for the desired 115 Vac or 230 Vac operating voltage. If 208 Vac operation is desired, select the 230 Vac position on the AC select switch, and change the power supplies transformer wiring by moving the space terminal from the '230' lug to the '208' lug on the primary.

(b) DC Operation Strapping. Follow the procedure in paragraph a. above and locate the A2A1 PWB. Follow the instructions adjacent to the terminal strip to configure the equipment for 12 Vdc or 28 Vdc operation. After terminal strip selection, return the equipment into the operate configuration as described above in paragraph a. Note that a different power cord configuration is also required for DC operation.

(2) Telephone Patch Strapping. The choices are 2 - wire, or 4 - wire telephone line interface. The internal 2 - wire/4 - wire hybrid select switch is located on the A1A16 Audio Interface PWB. The built-in telephone patch may be used with either 2 or 4 wire telephone circuits to permit telephone-to-radio communication. Selection of two or four wire operation is made via a switch located on the Audio Interface PWB, A1A16 (see figure 1-3 for location). To access this switch, remove the top cover of the transceiver, and locate the switch by the A1A16 assembly. Select the desired 2 - wire or 4 - wire position. Replace the top cover.

(3) CW Sideband Selection. The choices are CW-LSB or CW-USB. The switch for the CW Sideband Select is located on the A1A2 IF Filter PWB. Refer to figure 1-3 for the location of the A1A2 assembly.To set or check the setting of this switch, turn off power to 100 Watt Transceiver. Remove the top cover and locate the switch on the A1A2 assembly. Select the desired USB or LSB setting. Replace top cover. Turn power back on.

(4) AFSK Shift and Sideband Selection. The choices are AFSK-LSB or AFSK-USB, and AFSK 850 Hz, 170 Hz, or 85 Hz shift. To select the desired AFSK switch position, use the following procedure:

(a) Turn off 100 Watt Transceiver primary power switch.

2-4.

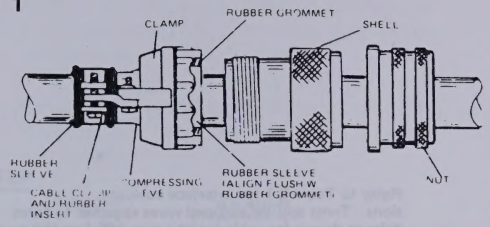
CAUTION

If the 28 Vdc power cable is connected to J6, equipment damage will occur.

c.

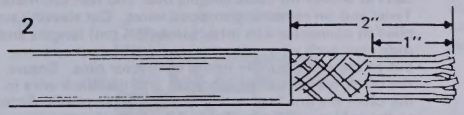
STEP

1



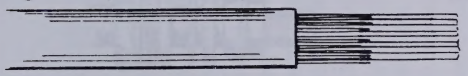
Install cable clamp and rubber insert, rubber sleeve clamp, compressing sleeve, rubber grommet, shell, and nut over cable. Assemble as shown. Leave cable clamp loose. Align rubber sleeve flush with rubber grommet inside clamp. Push assembly back out of the way to perform the steps shown below.

2



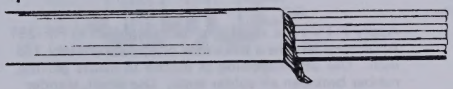
Remove 2" of vinyl jacket from cable as shown. Do not cut into shielding. Remove 1" of shielding as shown. Take care not to damage insulation on wires in cable bundle.

3



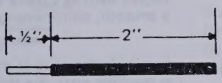
Carefully comb out shield wires as shown.

4



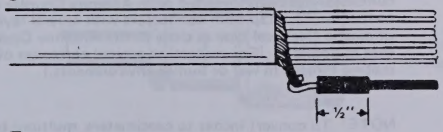
Make a part in the combed shield wires opposite the black wire in the cable. Pull the shield wires around both sides of the cable and twist together to make a pigtail as shown.

5



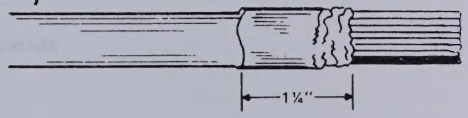
Remove 1/2" of insulation from a 2-1/2" length of No. 22 black stranded wire and tin.

6



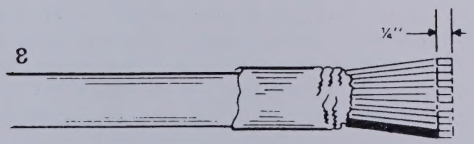
Twist the stripped end of black wire with the pigtail and solder. Cut 1/2" black shrink sleeving and install over soldered connection. Use a heat gun (an alternative is an open flame) to shrink sleeving exercising caution to avoid getting heat onto cable jacked.

7



Install shrink sleeving over cable as shown – apply heat and "shrink" in place. Use heat gun. If no heat gun is available use open flame. Avoid getting heat on cable jacket. Rotate cable for an even shrinkage.

8



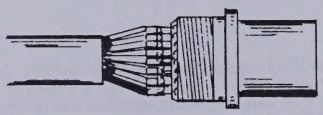
Remove ¼" insulation from wires to be used.

350-007

Figure 2-4. Typical Cable Fabrications (Sheet 1 of 3)

STEP

9.



Refer to Table 2-1 for interface connections. Twist and tin stripped wires together to form pairs as shown for cable lengths over 100 feet (30 meters). Twist and tin remaining stripped wires. Cut sleeving supplied in connector kits into ½ inch (1¼ cm) lengths and slide over each wire. Keep wires parallel as they come out of the cable bundle to the connector pins. Ensure the black wire installed in step 6 and the black wire in the cable are lined up with and soldered to pin D. Solder wires to the solder cups using Table 2-1. Slide sleeving over solder cups. Write down wire colors assigned to each pin number for reference when assembling the connector on the other end of the cable.

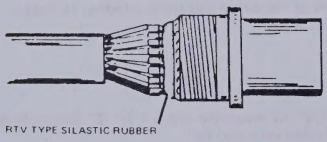
10.

Repeat assembly and soldering procedures for the other end of the cable.

11.

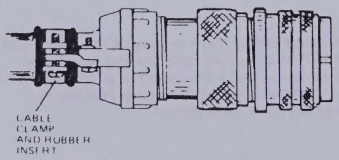
Check both ends of the cable for continuity, shorts between wires and shorts to the connector shell.

12.



Apply RTV type silastic rubber (supplied in RF-281 Accessory Kit) to a thickness of approximately 1/8 inch. Use small opening of nozzle to insure getting rubber between all solder cups. Use small, slender object such as a piece of wire or toothpick to insure a smooth, continuous waterseal.

13.

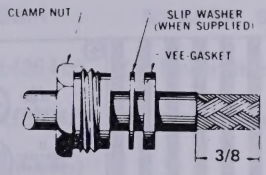
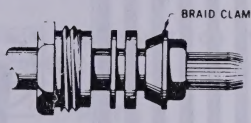
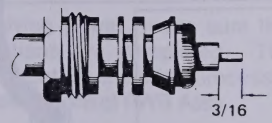
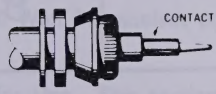
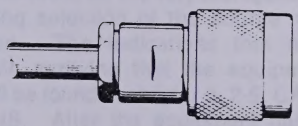


Assemble the plug as shown. Assemble clamp as tightly as possible onto the shell to assure a watertight connection around the cable. Repeat watersealing and assembling of connector on other end of cable. After connector has been threaded onto Antenna Coupler case connector J2, wrap both connectors with several layers of plastic electrical tape as close to the Antenna Coupler case as possible. (For protection against corrosion of mating threads in wet or humid environments.)

NOTE: To convert inches to centimeters, multiply by 2.540.

350-008

Figure 2-4. Typical Cable Fabrications (Sheet 2 of 3)

STEP		
1		Cut cable end square, place clamp-nut, slip washer (when supplied), and gasket over jacket. Remove 3/8" of vinyl jacket.
2		Place braid clamp over braid against jacket cut. Comb out copper braid as shown.
3		Fold braid back over braid clamp and trim as shown. Cut off dielectric 3/16" from end. Tin center conductor.
4		Solder contact to center conductor. Avoid use of excessive heat. See that end of dielectric is clean. Contact must be flush against dielectric. Outside of contact must be free of solder.
5		Thread assembly into connector, and lock securely. Vee gasket must be split by braid clamp.

350-009

Figure 2-4. Typical Cable Fabrications (Sheet 3 of 3)

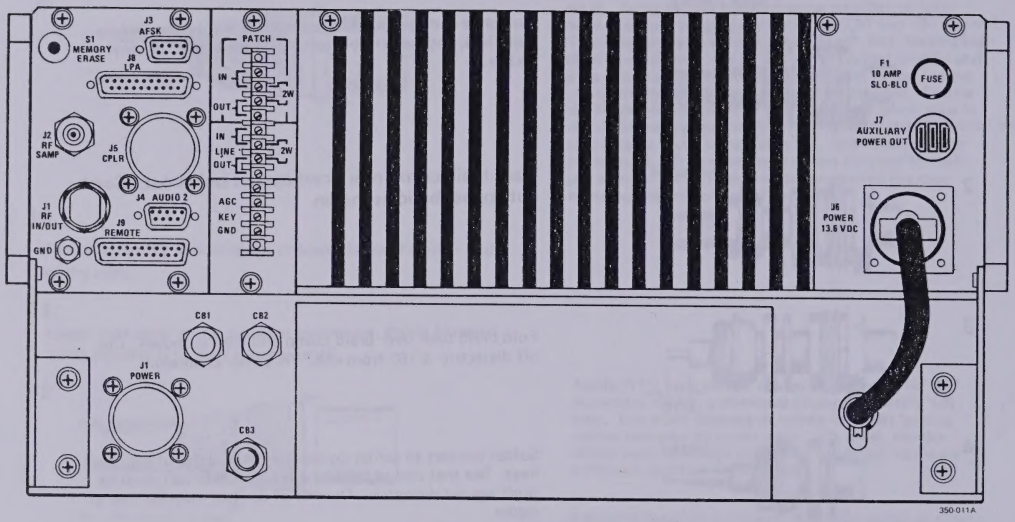


Figure 2-5. Rear Panel View, Connectors and Terminal Strip

(b) Remove top cover from 100 Watt Transceiver. Locate the AFSK IF Filter portion of the AFSK option as shown on figure 1-3. Refer to Chapter 6 if unfamiliar with disassembly of the 100 Watt Transceiver.

(c) Locate AFSK shift and sideband selection switches and select one of the following six combinations:

S1 - Shift	S2-AFSK Sideband
(1) 850 Hz (±425 Hz)	(1) Lower Sideband (LSB)
(2) 170 Hz (±85 Hz)	(2) Upper Sideband (USB)
(3) 85 Hz (±42.5 Hz)	

(d) Replace top cover on 100 Watt Transceiver.

NOTE

Before applying power, make sure that all interconnections are completed. This is necessary to set up the microprocessor on the Transceiver Control PWB Assy.

(e) Turn 100 Watt Transceiver power switch ON.

d. Preparation for Use. This section details the sequence of operations for the very first application of power, including selection of the source voltage switch position. The indications that may be expected, while verifying that the equipment is operational, will be found in chapter 3. 2-5. CABLING CONNECTIONS. After the equipment has been positioned and secured, fabricate and connect all cables to and from the 100 Watt Transceiver. If the use of the 100 Watt Transceiver involves only the supplied CW key, or Handset/Microphone, then the only cabling connections required are for the power and antenna cables. A power cord is supplied for the power connection. Cables must be fabricated by the user for most equipment applications. Cabling fabrication information is provided in figure 2-4 and table 2-1. Observe safety precautions in cable fabrication as detailed in figure 2-6.

NOTE

Cabling information for optional equipment (i.e., antenna coupler, LPA, etc.) is presented in Chapter 2 of each equipment's on-equipment manual. Refer to that manual for fabrication information.

2-5. INSTALLATION COMPLETE CHECK

a. Installation Verification. When the 100 Watt Transceiver has been installed with all connection cables attached, and is ready for the application of power, verify that each item in the list below has been completed.

(1) All connectors are attached and associated hardware is tight.

(2) Ground wires are connected between the 100 Watt Transceiver and a known good ground. Examples of a good ground are a cold water pipe, a long copper stake pounded into solid earth, or a system ground bus at an existing site.

(3) Check securing hardware to be sure the equipment can't be tipped over or moved.

(4) Check that area cooling is adequate for removing heat that may build up during equipment operation.

(5) Verify all strapping configurations as detailed in paragraph 2-4.

(6) Verify the power source is of adequate capacity and adequately protected for the 100 Watt Transceiver load, and that installation of the power cables is correct.

(7) Verify the antenna to be used is in place, correctly connected, and protected against accidental contact. If an antenna coupler is used, follow the guide lines in the antenna coupler documentation to be sure it is correctly installed.

(8) Check any companion equipment such as power supply, remote controls, power

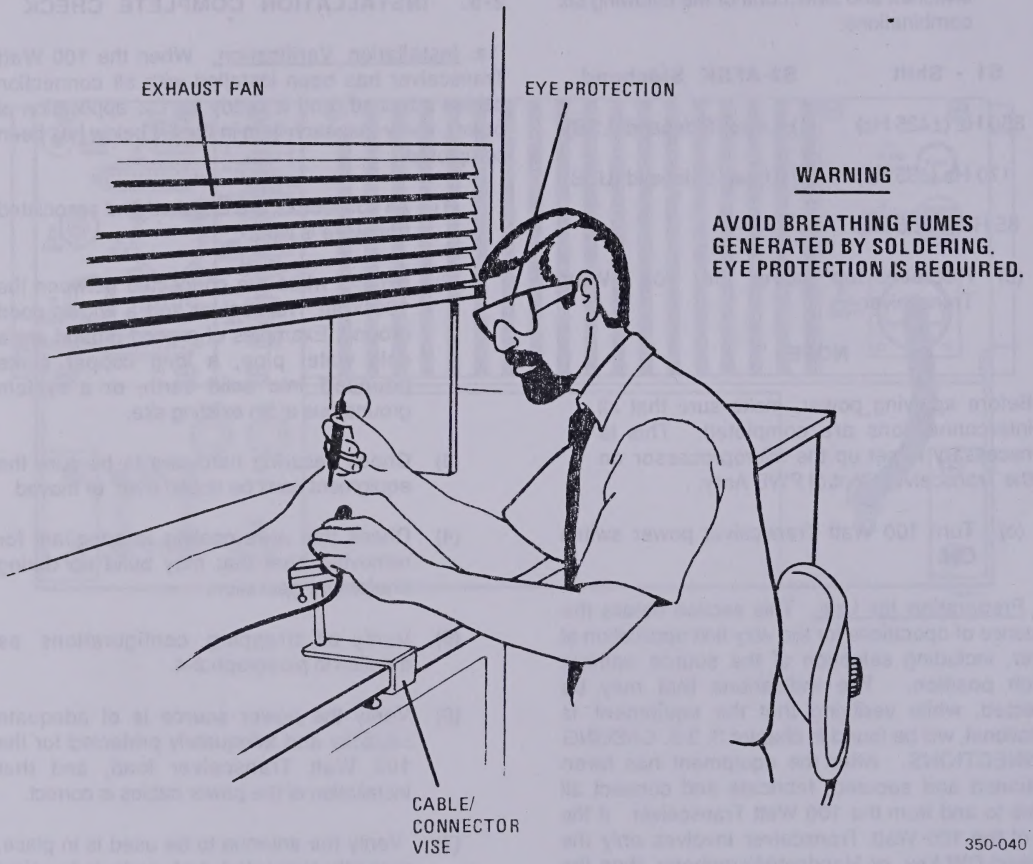


Figure 2-6. Safety Precautions for Fabrication of Cables

amplifiers, subordinate audio equipment, etc. for operational readiness.

b. Verification Testing. After each item on the list above has been checked, the equipment is ready for the application of power. Equipment testing sequences are discussed in Chapter 3 for the very first application of power. If the equipment does not require this sequence, proceed to chapter 4.

Table 2-1. 100 Watt Transceiver Interconnection Cabling

J1 RF In/Out (Coaxial)	
J2 RF Sample (Coaxial)	
J3 AFSK*	
J3-1	TX (-)
J3-2	AFSK Key (0V=Keyed)
J3-3	RX (+)
J3-4	Not Used
J3-5	Not Used
J3-6	TX (+)
J3-7	RX (-)
J3-8	Ground
J3-9	Not Used
J4 AUD2*	
J4-1	AUD2 PTT (0V=Keyed)
J4-2	RX Audio 0 dBm @ 600 ohm
J4-3	RX Audio 0 dBm @ 600 ohm
J4-4	TX Audio 0 dBm @ 600 ohm
J4-5	TX Audio 0 dBm @ 600 ohm
J4-6	Ground
J4-7	Not Used
J4-8	Not Used
J4-9	Not Used
J5 Coupler	
J5-A	Coupler Ground
J5-B	Coupler Key (0V=Keyed)
J5-C	Coupler Fault (0V=Fault)
J5-D	Coupler ID (0V=Coupler Connected)
J5-E	Tune Pulse (0V=Initiate Tune Cycle)
J5-F	Tune Power Request (0V=Request)
J5-G	Bypass (0V=Bypass)
J5-H	+13.6 VDC

* Do not rely on the pin identification numbers stamped on the body of chassis mounted "D" connectors J3 (AFSK) and J4 (AUDIO 2). The numbering sequence used may disagree with the in-line sequence dictated by the ribbon cable. When fabricating mating cables, always assume the numbering sequence shown in figure 2-7.

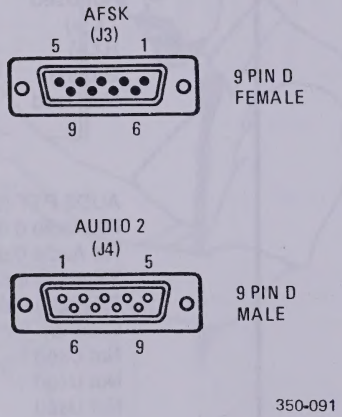


Figure 2-7. AFSK/AUD 2 Connectors: Pin Assignments

Table 2-1. 100 Watt Transceiver Interconnection Cabling (Continued)

J5-I	+13.6 VDC
J5-J	Key Disable (0V=Disable)
J5-K	LPA ID (0V=LPA Connected)
J5-L	115 VAC Line
J5-M	115 VAC Neutral
J5-N	Overtemp Fault (0V=Fault)
J6 Power	
J6-A	+12/28 VDC
J6-B	115/230 VAC Line
J6-C	Not Used
J6-D	+12/28 VDC Ground
J6-E	115/230 VAC Neutral
J6-F	Ground
J7 Auxiliary Power Out	
J7-1	+13.6 VDC
J7-2	FAN CONT + ON**
J7-3	Ground
J8 Linear Power Amplifier (LPA)	
J8-1	PPC Ground
J8-2	TGC (+)
J8-3	Ground (Vf, Vr)
J8-4	VFWD
J8-5	Data (+)
J8-6	LPA Key (0V=Keyed)
J8-7	LPA On/Off (0V=Off)
J8-8	Not Used
J8-9	Ground
J8-10	Not Used
J8-11	Not Used
J8-12	Not Used
J8-13	Not Used
J8-14	PPC
J8-15	TGC (-)
J8-16	VREFL
J8-17	LPA ID (0V=LPA Connected)
J8-18	Data (-)
J8-19	RF Mute (0V=Mute)

** Indicates that the signal is active low. On schematic diagrams, active low signals have a bar over the top.

Table 2-1. 100 Watt Transceiver Interconnection Cabling (Continued)

J8-20	Not Used
J8-21	Not Used
J8-22	Not Used
J8-23	Not Used
J8-24	Not Used
J8-25	Not Used
J9 Remote	
J9-1	N/C
J9-2	RS232 In
J9-3	RS232 Out
J9-4	RS422 (+) In
J9-5	RS422 (-) Out Aux
J9-6	RS422 (+) Out Aux
J9-7	Ground
J9-8	RS422 (-) In Aux
J9-9	RS422 (+) Out
J9-10	RS422 (+) In Aux
J9-11	Modem R (+)
J9-12	Line Out
J9-13	Line 2W/Line Out
J9-14	Ground
J9-15	Not Used
J9-16	RS422 (-) In
J9-17	Ground
J9-18	TXD (Aux)
J9-19	RXD (Aux)
J9-20	RS422 (-) Out
J9-21	Modem R (-)
J9-22	Modem T/R (-)
J9-23	Modem T/R (+)
J9-24	Line 2W/Line In
J9-25	Line In
TB1 Audio	
TB1-1	4-Wire Patch In -20 to 0 dBm @ 600 Ohm
TB1-2	4-Wire Patch In/2-Wire Patch In-Out
TB1-3	4-Wire Patch Out/2-Wire Patch In/Out -20 to 0 dBm @ 600 Ohm
TB1-4	4-Wire Patch Out
TB1-5	4-Wire Line In -10 dBm @ 600 Ohm
TB1-6	4-Wire Line In/2-Wire Line In-Out

Table 2-1. 100 Watt Transceiver Interconnection Cabling (Continued)

TB1-7	4-Wire Line Out/2-Wire Line In-Out -10 dBm @ 600 Ohm
TB1-8	4-Wire Line Out
TB1-9	Not Used
TB1-10	AGC Test
TB1-11	External PTT (0V=Keyed)
TB1-12	Ground
A2J1-A	+12/28 VDC
A2J1-B	115/230 VAC-L1
A2J1-C	Spare
A2J1-D	+12/28 VDC GND
A2J1-E	115/230 VAC-L2 (Neutral)
A2J1-F	Ground

2-6. SLIDE MOUNT INFORMATION

a. Slide Mounting and Brackets. This section shows general configuration and part pieces for Rack Mounting of Radios. Table 2-2, items 1 thru 7 are shown in illustration Figure 2-7, Items 8 and 9 are not shown, but are listed for reference purposes.

Table 2.2 Rack Mounting of Radios

ITEM	NOUN	PN	DESCRIPTION
1	Slide, left	C3307-234-L	Left hand slide assembly
2	Slide, right	C3307-234-R	Right hand slide assembly
3	Mount Bracket	4000-0252-CE	4 inch bracket for mounting slide
4	Mount Bracket	4000-0253-CE	8.5 inch bracket for mounting slide
5	Angle Bracket	10085-0062	5 inch stop bracket, RT-1446
6	Angle Bracket	10085-0362	3.5 inch stop bracket, RT-1446
7	Angle Bracket	10086-0062	7 inch stop bracket, AM-7223
8	Slide Set	10085-0207	Right/Left slide assembly set. Consists of above items 1 & 2.
9	Angle Bracket	10087-0062	10.5 inch stop bracket, AM-7224

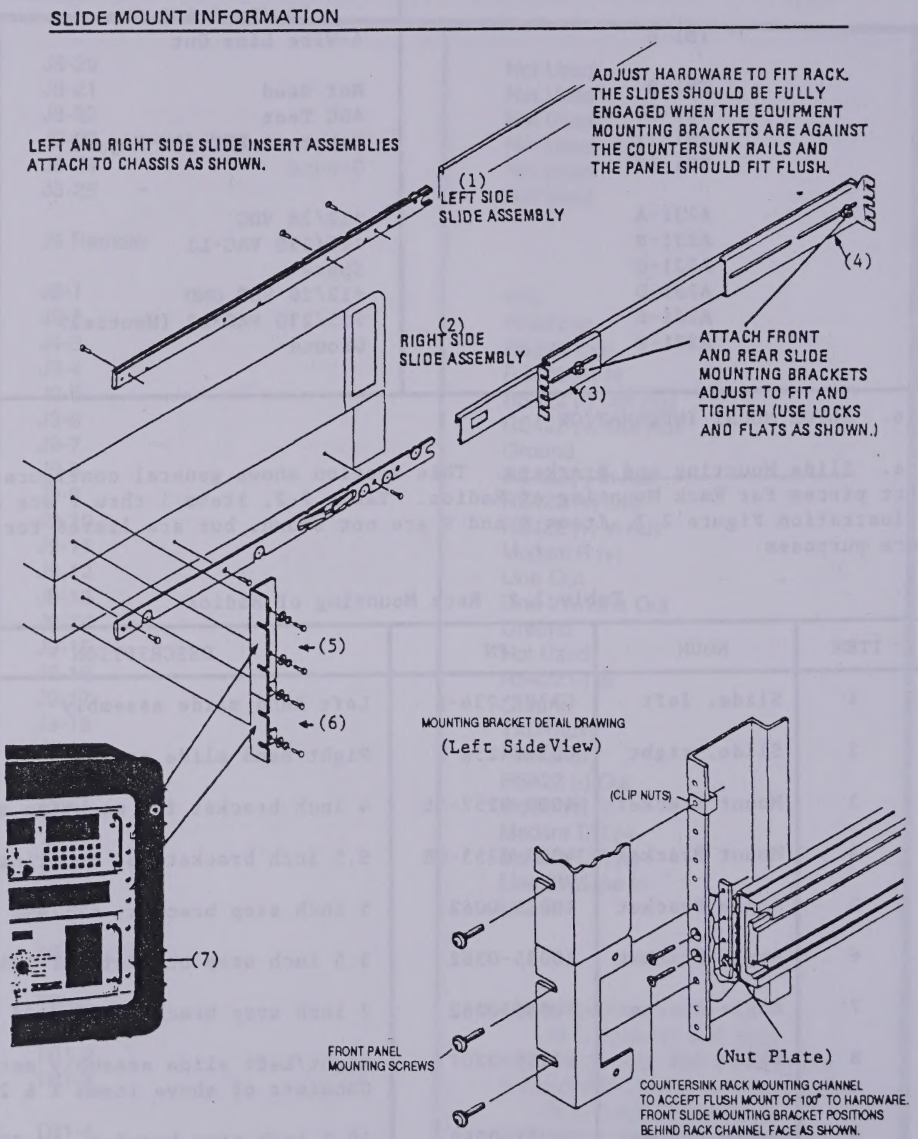

SLIDE MOUNT INFORMATION
ADJUST HARDWARE TO FIT RACK. THE SLIDES SHOULD BE FULLY ENGAGED WHEN THE EQUIPMENT MOUNTING BRACKETS ARE AGAINST THE COUNTERSUNK RAILS AND THE PANEL SHOULD FIT FLUSH.
LEFT AND RIGHT SIDE SLIDE INSERT ASSEMBLIES ATTACH TO CHASSIS AS SHOWN.
(1) LEFT SIDE SLIDE ASSEMBLY
(2) RIGHT SIDE SLIDE ASSEMBLY
(3)
(4)
ATTACH FRONT AND REAR SLIDE MOUNTING BRACKETS ADJUST TO FIT AND TIGHTEN (USE LOCKS AND FLATS AS SHOWN.)
(5)
(6)
(7)
MOUNTING BRACKET DETAIL DRAWING
(Left Side View)
(CLIP NUTS)
(Nut Plate)
FRONT PANEL MOUNTING SCREWS
COUNTERSINK RACK MOUNTING CHANNEL TO ACCEPT FLUSH MOUNT OF 100° TO HARDWARE. FRONT SLIDE MOUNTING BRACKET POSITIONS BEHIND RACK CHANNEL FACE AS SHOWN.

Figure 2-7. Slide Mount and Bracket Information.

CHAPTER 3

PREPARATION FOR USE AND RESHIPMENT

WARNING

Dangerous voltages exist in this radio equipment.
Before removing any cover, disconnect primary power.

Section I. PREPARATION FOR USE

3-1. INITIAL CONTROL SETTINGS. This section details the initial control settings prior to the application of power to the 100 Watt Transceiver. These control settings are listed in table 3-1. Note that all controls are on the front panel of the 100 Watt Transceiver; companion equipment controls will not be discussed. It is assumed that the 100 Watt Transceiver is fully installed and correctly connected as described in chapter 2 of this manual. If in doubt about the installation of the 100 Watt Transceiver, verify the information in chapter 2 before proceeding.

Table 3-1. Initial Control Settings

Control	Initial Setting
1. Power (POWER)	Select OFF position.
2. Speaker (SPKR)	Select ON position.
3. Squelch (SQUELCH)	Select OFF (fully counterclockwise into the detent position).
4. Audio (AUDIO)	Select minimum gain (fully counterclockwise position).
5. RF Gain (RF GAIN)	Select maximum gain (fully clockwise position)

3-2. INITIAL POWER APPLICATION. This portion of the manual provides a step-by-step sequence for the initial application of power to the 100 Watt Transceiver. The selection of a keypad push button is shown in brackets. For example, selection of the MODE key is shown as [MODE]. Two sequential keystrokes would be shown as, for example, [2ND][VOX], where [2ND] is pressed, and then [VOX] is pressed.

3-3. SEQUENCE FOR POWER-UP. The step-by-step power-up sequence provided below assumes a general application configuration and does not include the use of ancillary equipment.

a. Step-by-Step Sequence for Initial Power Application.

(1) Connect A1J1 RF INPUT/OUTPUT to a proper 50 ohm antenna, or antenna coupler if the antenna does not exhibit a 50 ohm load. Be sure the antenna power handling capacity is adequate for the equipment configuration, and transmissions will not present a danger to nearby personnel.

(2) Place 100 Watt Transceiver POWER switch into the POWER ON position.

(3) Observe the following frequency and mode status at the front panel LCD displays:

Frequency:	10,000.00 KHz
Mode:	MODE: USB
AGC:	AGC: SLOW
Audio Input:	AUDIO: MIC
Meter:	FWD
Local/Remote:	Local (there is no display for Local)

NOTE

If the equipment has been operated previously, the display will show the last frequency, mode, etc. that was in use by the 100 Watt Transceiver at power off. The display status listed above represents the "default" configuration when there is nothing in the parameter memory device. The "default" display indicates that the memory feature has no stored information. The memory feature is powered by an internal lithium battery during periods when no primary power is applied to the equipment. The battery has a projected life of 10 years. If a FAULT condition or no display is observed, the equipment may be inoperable. In such case, refer to the corrective maintenance information in chapter 6. Also, observe at initial application of primary power that the cooling fan is operating at low speed. The fan will automatically switch to high speed when an internal detector determines the equipment has reached a temperature that requires more rapid cooling. After the equipment has cooled, the fan automatically switches to low speed.

(4) Press [2ND][TEST]. Observe all front panel LCD segments are turned on, followed by a readout in the frequency field indicating PASSEd.

NOTE

Remove power, then remove antenna-connection (remove all connections to antenna coupler if so configured), attach dummy load to power connection of radio and repeat test before further maintenance action.

- To confirm that all the LCD segments are illuminated, refer to chapter 4 for a description of the display. Pressing [2ND] [TEST] invokes the BIT (Built In Test) feature. All modules in the receive signal path are functionally tested, and if no faults are discovered, the PASSEd display is indicated. If a fault is discovered, the reference designator of the assembly causing the fault will be displayed in the frequency field. Any fault indication should be analyzed before proceeding. Refer to chapter 6, maintenance, if a fault indication occurs.

(5) Press [2ND][TX KEY][2ND][TEST]. Observe a readout in the frequency display PASSEd. When procedure is complete, press [2ND][TX KEY] to unkey transmitter.

NOTE

If an antenna coupler is attached, a previous tune cycle is required before you execute the transmit BIT test.

CAUTION

This sequence automatically keys the 100 Watt Transceiver to functionally test the transmit signal path. Since you will be transmitting on the displayed frequency, make sure that this frequency is authorized for operation before testing. Be sure a dummy load is connected and transmissions will not pose a danger to personnel. All modules in the transmit path are tested, and if no faults are discovered, the PASSEd display is indicated. If a fault is discovered, the reference designator of the assembly causing the fault will be displayed in the frequency field. Any fault indication should be analyzed before proceeding. Refer to chapter 6, Maintenance, if a fault indication occurs.

b. When Indications are Normal. If indications are normal, proceed to paragraph 3-4.

3-4. INITIAL CHECKOUT. Do not change the configuration of the 100 Watt Transceiver that was used in paragraph 3-3, i.e., the antenna load should remain connected. The checkout procedure is organized in step-by-step sequence as provided below and should be conducted immediately after performing the initial power application in paragraph 3-3.

NOTE 1

This sequence does not cover each feature or function of the 100 Watt Transceiver. Refer to the Chapter 4, Operation, for detailed operation information. In addition, the features related to the use of companion equipment are not discussed, e.g., Remote Control, Linear Power Amplifier (LPA), AFSK, etc. Refer to the appropriate instructions for these units.

NOTE 2

This sequence assumes the 100 Watt Transceiver is being powered for the first time. If this is not the case, some indications in this sequence will reflect information previously stored in the 100 Watt Transceiver memory. It is possible to erase the entire memory by activation of the MEMORY ERASE button at the rear panel of the 100 Watt Transceiver. The 100 Watt Transceiver will then respond as if it were powered for the first time. However, this should be done only with a clear understanding of the consequences, i.e., all channel information is erased, and all last parameter information is erased.

a. Prepare Display for Initial Checkout.

(1) If the BIT test of paragraph 3-3 have been completed successfully, the display will indicate PASSEd.

(2) If the REMOTE indicator is illuminated, select LOCAL by pressing [2ND][REMOTE].

b. Check FREQUENCY Function - Numeric Key Method.

(1) Press [FREQ]. Observe the word FREQ displayed in the LCD frequency field, and that the 10 MHz digit is blinking.

(2) Load 12,345.67 KHz in display with keypad. Note that following the keying of each number, the next digit position blinks.

NOTE

Additional digits will re-enter in display allowing correction or re-entry.

(3) Press [ENTER].

(4) Observe 12,345.67 is displayed in LCD frequency field, no digits are blinking, and the word FREQ is no longer displayed.

c. Check FREQUENCY Function - Up/Down Increment Method.

(1) Press [FREQ]. Observe the word FREQ displayed in the LCD frequency field.

(2) Push [SCROLL UP] and observe the frequency changes upward in 10 Hz steps.

(3) Release [SCROLL UP]. Observe frequency display is fixed at some higher frequency.

(4) Press [FREQ] and observe the word FREQ displayed in the LCD frequency field.

(5) Press [SCROLL DOWN]. Observe the frequency changes downward in 10 Hz steps.

(6) Release [SCROLL DOWN]. Observe the frequency display is fixed at some lower frequency.

(7) Use [SCROLL UP][SCROLL DOWN] to select a frequency 12,345.67 KHz.

d. Check MODE Function.

(1) Press [MODE] and observe the MODE indicator scrolls through the modes, USB, LSB, AME, CW,and AFSK (with option).

NOTE

When a MODE is selected, an AGC speed is automatically selected. In USB, LSB, or CW modes, AGC: SLOW is automatically selected. In AME or AFSK modes, AGC: FAST is automatically selected. The AGC speed can be changed, as described in Step i. of this procedure.

(2) Scroll [MODE] to USB.

e. Check CHANNEL Function - Numeric Key Method.

(1) Press [CHAN] and observe the word CHAN displayed in the LCD channel field.

(2) Enter "50" in display with keypad.

NOTE

Additional digits will re-enter in display allowing correction or re-entry.

(3) Press [ENTER] when the display is correct.

(4). Observe "50" is displayed in LCD channel field and any existing programmed parameters displayed.

(5) Press [FREQ][ENTER] and observe the

channel feature is cleared.

f. Check CHANNEL Function - Up/Down Increment Method.

(1) Press [CHAN] and observe the word CHAN displayed in the LCD channel field.

(2) Press [SCROLL UP] and observe the channel number increments at one second intervals.

(3) Release [SCROLL UP]. Observe channel display is fixed at some higher channel. It is not necessary to use [ENTER] in this method.

(4) Press [SCROLL DOWN] and observe the channel number decrements at one second intervals.

(5) Release [SCROLL DOWN]. Observe channel display is fixed at some lower channel. It is not necessary to use [ENTER] in this method.

(6) Press [FREQ][ENTER] and observe that the channel feature is cleared.

g. Check CHANNEL Function - Test Program a Channel.

(1) To test program a channel, press [2ND][PROG] and observe the CHAN indicator illuminates, and all front panel indicators except displayed frequency and MODE are turned off.

(2) Enter the channel number 50 into the channel display, followed by [ENTER]. Previous channel 50 frequency and mode of operation programming will be displayed for channel 50 (if any).

(3) Load the frequency information 23,456.78 KHz into the FREQ display, via the numeric keys, then scroll [MODE] to CW. Press [2ND][LOAD].

(4) Observe the channel program process is terminated and the display returns to the operating conditions that were set before programming started, or to the default parameters.

(5) Verify the channel memory feature by calling up channel 50 by following step e. above. When channel 50 is verified (23,456.78 MHz, CW mode), press [FREQ][ENTER] to exit the channel feature.

h. Check BFO Function.

(1) Press [BFO] and observe the word BFO displayed in the LCD frequency field. Above (+) or below (-) BFO indications may also be present.

(2) Press [SCROLL UP] and observe the BFO center frequency increases above center frequency as shown by the (+) indicator.

NOTE

The BFO frequency (0 to ±1 KHz) changes in 10 Hz steps but the BFO frequency is not displayed. Only a (+) or (-) symbol is indicated.

(3) Push [SCROLL DOWN] until the BFO frequency is centered again. Then continue until the (-) indicator is observed.

(4) Center the BFO and press [BFO][BFO] to exit BFO function.

i. Check AGC Function.

(1) Press [AGC] and observe the AGC indicator scrolls from SLOW to MED. Press [AGC] again and observe a change from MED to FAST. Press and hold [AGC] and observe it scrolls through the three AGC speeds, SLOW, MED, and FAST. Scroll to AGC FAST.

(2) Press [2ND][AGC OFF] and observe AGC OFF is displayed and AGC FAST is no longer displayed.

(3) Press [AGC] and observe AGC OFF is no longer displayed and AGC FAST illuminates.

NOTE

When going from AGC OFF to AGC, the readout is always AGC: SLOW when in the USB and LSB modes, and AGC: FAST in the

AME and AFSK modes. In the CW mode, the AGC speed selected before the AGC was turned off appears in the display.

j. Check Audio Source Function (must be in USB, LSB or AME mode).

(1) Press [AUDIO SOURCE] and observe it scrolls through the three audio source positions.

(2) Stop at AUDIO: MIC.

k. Check Meter Input Function.

(1) Press [METER] and observe the METER scale changes from FWD to REF (S- scale).

(2) Continue to press [METER] and observe that the meter scale scrolls through the following positions:

(a) FWD - S-scale, received signal strength (unkeyed)

(b) REF - S-scale, received signal strength (unkeyed)

(c) VSWR-S-scale, received signal strength (unkeyed)

(d) AUDIO - Relative TX audio from all sources (keyed)

(e) LINE - Line audio (keyed or unkeyed)

(f) PATCH - Patch audio (keyed or unkeyed)

(g) AFSK - Audio Frequency Shift Center Freq (must be in AFSK mode).

(3) Scroll to the FWD meter indication.

l. Check VOX Function.

(1) Press [2ND] [VOX] and observe the VOX: VOICE indicator illuminates.

(2) Press [2ND] [VOX] again and observe the display VOX: DATA.

(3) Press [2ND] [VOX] again and observe the VOX display is not lit (VOX disabled).

m. Check AFSK Signal Inversion Function.

NOTE

Conduct step m only when AFSK option is installed.

(1) Select the AFSK mode (see step d.).

(2) Press [2ND] [FSK REV]. Observe that the CREV (Converter Reverse) indicator illuminates.

(3) Press [2ND] [FSK REV] to scroll through the positions of CREV (Converter Reverse), and KREV (Keyer Reverse) combinations shown in the sequence below. Note: There is no display for Normal sense.

(a) Normal - CREV

(b) KREV - Normal

(c) KREV - CREV

(d) Normal - Normal

(4) Select the USB mode.

n. Check CLIP Function.

(1) Press [2ND] [CLIP]. Observe the CLIP indicator illuminates (audio source to MIC).

(2) Press [2ND] [CLIP] again, and observe that the CLIP indicator extinguishes.

o. Check Transmitter Operation.

CAUTION

Verify before proceeding that the J1 RF INPUT/OUTPUT jack is connected to a dummy load with adequate capacity before proceeding.

(1) Select frequency 12,345.67 KHz (step b.).

(2) Connect the CW key to the front panel and select CW mode (step d.).

(3) Select Meter input FWD (Forward Power) (step k.).

(4) Press the CW key. Observe the transmitter has an output by observing that the Meter Scale reading is100 watts (nominal) and that the XMIT indicator iluminates.

(5) With the transmitter still keyed, observe a steady tone from the front panel speaker.

(6) Press [2ND] [S TONE] and observe that the steady tone stops.

(7) Release the CW key and observe that the meter indication drops to zero and XMIT indicator is no longer illuminated after a slight delay.

(8) Remove the CW Key and connect the Handset/Mic to the front panel connector.

(9) Select USB mode (step d.).

(10) Select Audio Source MIC (step j.).

(11) Key the transmitter by pressing the push-to-talk button on the Handset/Mic. During the key down condition, observe that the XMIT indicator is illuminated. While keying, talk normally into the microphone and observe that on voice peaks, the FWD meter scale reads approximately 100 watts.

(12) Repeat steps (9), (10), and (11) above for the LSB and AME modes. Remove the Handset/Mic.

NOTE

At any time during the above step, the internal 100 Watt Transceiver cooling fan may automatically switch to high speed. In AME mode testing, RF power output is 25 watts without modulation.

p. Check Receiver Operation.

(1) With the unit connected to an antenna, perform the following checks.

(2) Adjust the frequency (see step b.) and mode (see step D) controls for reception of a known currently active communications channel. Adjust the AUDIO for a comfortable listening level.

(3) Select the SPKR switch OFF position and observe the 100 Watt Transceiver speaker audio is turned off. Connect headset at front panel and verify audio is present.

(4) Select the SPKR switch ON position and observe the 100 Watt Transceiver is turned on. Disconnect headset.

(5) Turn the RF GAIN control slowly counterclockwise and observe the gradual desensitizing of the receiver. Return the RF GAIN control to the full clockwise position.

(6) Turn the SQUELCH control slowly clockwise (out of the detent position) and observe at some point the received audio is squelched. Return the SQUELCH control to the full counterclockwise position (into detent).

NOTES

If the received radio signal is very strong, the100 Watt Transceiver will not squelch. If this is the case, retune the 100 Watt Transceiver to a weaker radio station and repeat (6) above.

It is normal for some sound to still be heard in the speaker when the 100 Watt Transceiver is in squelch. This is a feature to allow some audio feedback to an operator rather than unsquelching the receiver to check for signal presence.

(7) Select the CW Mode. Tune in a station operating in CW or transmitting a partial carrier. To change tone, press the BFO control and follow step h. Clear the BFO feature by pressing [BFO][BFO].

(8) Turn 100 Watt Transceiver Power Switch to the POWER OFF position.

q. End of Test. This completes the initial check-out procedure. If any difficulties were encountered, refer to maintenance, chapter 6. Minor adjustments to bring performance into the normal range of values are included in the procedures in chapter 4, operation.

Section II. PREPARATION FOR RESHIPMENT

3-5. PREPARATION FOR RESHIPMENT. Reshipment of the 100 Watt Transceiver is accomplished by reversing the sequence described in paragraph 2-1 and illustrated in figure 2-1. There are no special dismantling or disassembly requirements. It is assumed that the original shipping container was retained. Remove the 100 Watt Transceiver from the rack, equipment stack, etc., and place into the container. It is not necessary to remove any 100 Watt Transceiver special plug-in-units or assemblies. The container packing surrounds the equipment for shock protection. The packed carton should be securely bound with reinforced tape or metal bands for reshipment.

CHAPTER 4

OPERATION

WARNING

Dangerous voltages exist in this radio equipment.
Before removing any cover, disconnect primary power.

Section I. CONTROLS AND INDICATORS

4-1. CONTROL AND INDICATOR DESCRIPTIONS. All 100 Watt Transceiver controls and indicators are shown in figure 4-1. Control and indicator functions are explained in table 4-1.

4-2. TRANSCEIVER KEYPAD CONTROL. Most 100 Watt Transceiver control functions are selected via a front panel digital keypad. Keypad selections are entered into memory for use by the microprocessor. The numeric and scroll keys have dual functions. To select the key's second function, the 2ND key is pressed first, and then the dual function key. Note that when a key or a key dual function is mentioned, brackets are used around the name of the key(s); e.g., [2ND][LOAD] indicates sequential operation of the 2ND key, then the LOAD key.

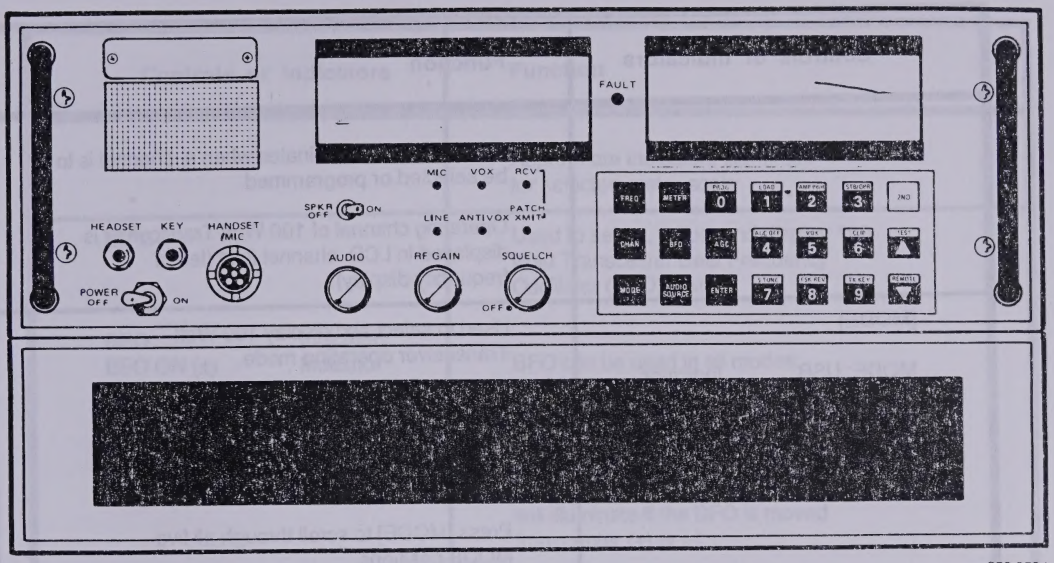
NOTE

To prevent damage to the vinyl keypad cover, use fingers only to depress keys.

4-3. OPERATING INSTRUCTIONS. For specific information regarding the operating instructions of the 100 Watt Transceiver controls and indicators, see section II of this chapter.

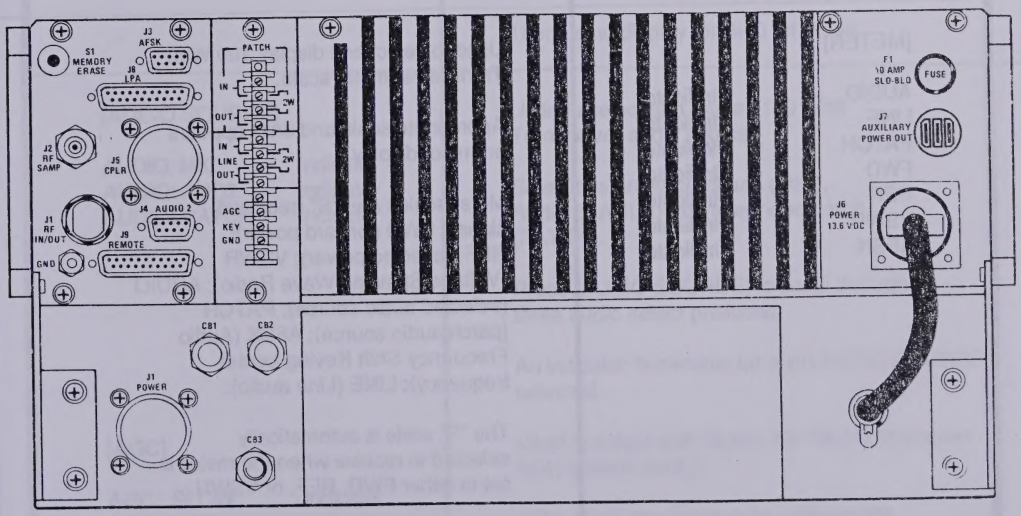
Table 4-1. 100 Watt Transceiver Operating Controls and Indicators

Controls or Indicators	Function
[FREQ] FREQ Indicator	Used to select a 100 Watt Transceiver operating frequency. [FREQ] is pressed, followed by frequency information with numeric keys [0-9], then [ENTER]. Minimum entry is 01,600.00 KHz. Maximum entry is 29,999.99 KHz. FREQ indicator illuminates only when a frequency is to be entered. Operating frequency of 100 Watt Transceiver is displayed in LCD frequency field.
[CHAN] CHAN Indicator	Used to select a 100 Watt Transceiver operating channel. [CHAN] is pressed, followed by channel information with numeric keys [0-9], then [ENTER]. Minimum entry is channel 00. Maximum entry is channel 99.



350-059A

FRONT PANEL



REAR PANEL

Figure 4-1. 100 Watt Transceiver Operating Controls and Indicators

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	CHAN indicator illuminates when a channel is to be selected or programmed. Operating channel of 100 Watt Transceiver is displayed in LCD channel field (left of frequency display).
[MODE] MODE: USB Indicator MODE: LSB Indicator MODE: AME Indicator MODE: CW Indicator MODE: AFSK Indicator	Used to select and display 100 Watt Transceiver operating mode. Modes are Upper Sideband (USB), Lower Sideband (LSB), Amplitude Modulation Equivalent (AME), CW (Morse), and Audio Frequency Shift Keying (AFSK). Press [MODE] to scroll through all five MODE positions. Appropriate MODE indicator illuminates for selected position. Indicator MODE: AFSK illuminates only if AFSK option is installed.
[METER] AUDIO Indicator LINE Indicator PATCH Indicator FWD Indicator REF Indicator VSWR Indicator AFSK Indicator	Used to select and display 100 Watt Transceiver meter scale. Appropriate scale and units appears on meter display. Meter scales are; "S" (received signal); FWD (forward power); REF (reflected power); VSWR (Voltage Standing Wave Radio); AUDIO (selected audio source); PATCH (patch audio source); AFSK (Audio Frequency Shift Keying center frequency); LINE (Line audio). The "S" scale is automatically selected in receive when the meter is set to either FWD, REF, or VSWR. Press [METER] to scroll through seven meter positions.

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	Appropriate indicators illuminate for selected meter scale.
[BFO] BFO Indicator BFO ON (±) Indicator	Used to select, adjust and display 100 Watt Transceiver Beat Frequency Oscillator (BFO) feature. BFO can be used in all modes. Press [BFO] to toggle between BFO on and off. BFO indicator will illuminate BFO ON (±), showing BFO position in relation to center (no offset), and will illuminate if the BFO is moved from center (+) or (-). In BFO mode, [SCROLL UP][SCROLL DOWN] alters the BFO frequency by 10 Hz per keystroke. Hold scroll key down for multiple 10 Hz increment entry. There is no readout of BFO frequency. There is no display for BFO off mode.
[AUDIO SOURCE] AUDIO: MIC Indicator AUDIO: AUD2 Indicator AUDIO: PATCH Indicator [AGC] AGC: SLOW Indicator AGC: MED Indicator AGC: FAST Indicator	Used to select and display 100 Watt Transceiver audio source. Selections are Microphone (MIC), Audio 2 (AUD2) and telephone patch (PATCH). Press [AUDIO SOURCE] to scroll through three audio select positions. An indicator illuminates for each AUDIO SOURCE selected. Used to select and display 100 Watt Transceiver AGC speed (decay). AGC attack time fixed at 30 milliseconds. Decay times are: 3 ±1 second (AGC:SLOW),

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	200 ± 100 milliseconds (AGC: MED) and 30 milliseconds or less (AGC: FAST). Press [AGC] to scroll through three AGC speeds. An indicator illuminates for AGC speed selected. [AGC] does not function if AGC: OFF is displayed. (See [AGC OFF]/[4]).
[ENTER]	Used in conjunction with frequency and channel keys to enter information into 100 Watt Transceiver memory.
[PROG]/[0]	Used in programming Channel feature; also used as numeric [0]. Press [2ND][PROG] to select programming feature.
[LOAD]/[1]	Used with Channel feature to load programming into memory; also used as numeric [1]. Press [2ND][LOAD] to place channel programming into memory.
[AMP PWR]/[2] LPA MAN Indicator AMP: Indicator	Used to control and display Power Supply status for a companion Linear Power Amplifier (LPA); also used as numeric [2]. Press [2ND][AMP PWR] to select LPA power supply on and off. LPA must be in AUTO for [AMP PWR] to function (LPA AUTO is selected at LPA front panel). When Linear Power Amp is on, AMP:STBY indicator illuminates and flashes during 3 minute warm-up period. After warm-up, flashing stops.

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	If LPA is in Manual mode, LPA MAN indicator illuminates, and [AMP PWR] has no effect.
[STB/OPR]/[3] AMP: STBY Indicator AMP: OPER Indicator	Used to control and display Standby or Operate status for a companion Linear Power Amplifier (LPA); also used as numeric [3]. Press [2ND][STB/OPR] to toggle LPA between Operate and Standby conditions. Flashing indication AMP: STBY occurs during 3 minute warm-up period for LPA. Indicator not flashing occurs when warm-up period is over. Any display of AMP: STBY places LPA in bypass and it is transparent to 100 Watt Transceiver operation. Indicator AMP: OPR flashes when LPA requires tuning. Indicator not flashing indicates when LPA is tuned and ready for operation. The AMP: OPR tune cycle is initiated by keying 100 Watt Transceiver. If AMP: OPER indicator is illuminated and 100 Watt Transceiver is keyed, [STB/OPR] has no effect until keyline is removed.
[AGC OFF]/[4] AGC: OFF Indicator	Used to select and display 100 Watt Transceiver Automatic Gain Control (AGC) OFF function. Also used as numeric [4]. Press [2ND][AGC OFF] to select AGC OFF. When AGC OFF is selected, AGC OFF indicator illuminates. The AGC ON is reenabled via the [AGC] key.
[VOX]/[5] VOX: VOICE Indicator VOX: DATA Indicator	Used to select and display 100 Watt Transceiver Voice Operated Transmit (VOX) feature; also used as numeric [5]. VOX modes are VOX: DATA, VOX: VOICE, and VOX OFF.

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	Press [2ND][VOX] to scroll through VOX modes. When VOX feature is active, VOX: VOICE or VOX: DATA illuminates. VOX OFF has no display.
[CLIP]/[6] CLIP Indicator	Used to select and display 100 Watt Transceiver transmit peak audio clipping function (CLIP); also used as numeric [6]. Press [2ND][CLIP] to toggle between CLIP on and off modes. When CLIP on is active, CLIP indicator illuminates. CLIP is selectable only in USB, LSB, and AME modes. CLIP level is adjustable internal to 100 Watt Transceiver.
[S TONE]/[7]	Used to select Sidetone (S TONE) feature; also used as numeric [7]. Press [2ND][S TONE] to toggle between on and off modes. Sidetone is selectable in voice modes, and is automatically selected in the CW mode. There is no front panel indicator for sidetone.
[FSK REV]/[8] AFSK CREV Indicator AFSK KREV Indicator	Used to select and display sense of AFSK keyer/converter; also used as numeric [8]. CREV identifies Converter Reverse, and KREV identifies Keyer Reverse. Press [2ND][FSK REV] to scroll through four combinations:

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	Converter / Keyer / Display 1. Normal / Reverse / "KREV 2. Reverse / Normal / CREV 3. Reverse / Reverse / KREV/CREV 4. Normal / Normal / (none) Only CREV and KREV selections have indicators. AFSK mode selects AFSK portion of indicator. AFSK option must be installed for [FSK REV] to function. Normal sense is consistent with MIL-STD-188-114 where (+) = binary 0 = space; (-) = binary 1 = mark.
[TX KEY]/[9] XMIT Indicator TUNE Indicator	Used to key 100 Watt Transceiver to initiate tune sequence, to perform support operations, etc.; also used as numeric [9]. Press [2ND][TX KEY] to toggle keyline on and off. When transmitter is keyed, XMIT indicator illuminates. If a companion antenna coupler is used, TUNE indicator illuminates during antenna coupler tune cycles. At end of antenna coupler tune cycle, TUNE indicator extinguishes. Antenna Coupler tune sequencing is automatic.
[TEST]/[SCROLL UP]	Used to command Built-in Test (BIT) self-test feature; also used as [SCROLL UP]. Press [2ND][TEST] to initiate receiver self-test feature. At end of a successful test, word "PASSEd" appears in frequency display. Press [2ND][TX KEY][2ND][TEST] to initiate receiver and transmitter self-test feature. At end of a successful test, word PASSEd appears in frequency display.

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
	NOTE At the end of the test, the radio is still keyed. Press [2ND] [TX KEY] to unkey the system. If a fault is detected with BIT, frequency display indicates which assembly failed. [SCROLL UP] function is used for frequency, channel and BFO entries.
[REMOTE]/[SCROLL DOWN] REMOTE Indicator	Used to select and display Remote Control mode; also used as [SCROLL DOWN] Press [2ND][REMOTE] to toggle between remote and local mode. REMOTE indicator illuminates in remote mode. There is no indicator for local mode. [SCROLL DOWN] selection is used for frequency, channel and BFO entries.
[2ND]	Used to select second function of dual function keypad pushbuttons. [0] through [9], [SCROLL UP] and [SCROLL DOWN] have dual functions. Press [2ND] then function to select.
FAULT Indicator LOW PWR Indicator BYPASS Indicator	Used to indicate a 100 Watt Transceiver failure or reduced performance condition. FAULT indicator illuminates when a failure occurs. Press [2ND][TEST] to reveal source of failure. FAULT light also illuminates when a companion LPA fails. LOW PWR indicator illuminates if RF output power of 100 Watt Transceiver drops below a preset

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators		Function
		level (approximately 50 watts). Will illuminate several seconds after unit is keyed if no power output is present. BYPASS is a fault indicator that illuminates when the 100/500 Watt Antenna Coupler is unable to tune. In bypass, the antenna system bypasses the 100/500 Watt Antenna Coupler and is connected directly to the 100 Watt Transceiver. The 100 Watt Transceiver may transmit in bypass, however, RF power output may automatically be reduced, if required, to prevent 100 Watt Transceiver damage.
SPKR	Switch	Used to turn front panel speaker on and off. Front panel speaker is automatically disconnected if the supplied handset is connected to the front panel HANDSET/MIC jack.
AUDIO	Control	Used to set front panel speaker and headphone audio level.
POWER	Switch	Used to switch 100 Watt Transceiver primary power on and off.
RF GAIN	Control	Used to vary sensitivity of receiver.
SQUELCH	Control	Used to adjust SQUELCH threshold level allowing only signals exceeding threshold to be monitored.
MIC	Control	Used to adjust microphone gain level.
LINE	Control	Used to adjust received audio level for the line output.

Table 4-1. 100 Watt Transceiver Operating Controls and Indicators (Continued)

Controls or Indicators	Function
PATCH XMIT Control PATCH RCV Control	Used to adjust patch audio input and output levels.
VOX Control ANTIVOX Control	Used to adjust Voice Operated Transmit (VOX) feature. VOX adjustment sets threshold of audio level required to trigger VOX keyline output. ANTIVOX adjustment counteracts receiver audio output in VOX circuit to prevent false VOX operation.
MEM ERASE Control	Used to erase entire 100 Watt Transceiver temporary (RAM) memory. Erases all preset channels, all last operating parameters, etc. Control is located on rear panel of 100 Watt Transceiver. Normally used in a security situation where memory in unattended 100 Watt Transceiver is erased to prevent unauthorized disclosure of operating frequencies and parameters.

Section II. OPERATING INSTRUCTIONS

4-4. INTRODUCTION. Operating instructions include those for the 100 Watt Transceiver and for companion equipment that are controlled via the 100 Watt Transceiver. Refer to the associated technical manuals for any companion equipment such as linear power amplifiers and antenna couplers for detailed discussion of operation procedures. Since the 100 Watt Transceiver can be operated with a variety of ancillary equipment, it is the responsibility of the user to configure the equipment to support the intended operations. If the 100 Watt Transceiver is operated with a companion Remote Control equipment, refer to the Remote Control chapter for selecting remote operation as these procedures assume local operation.

4-5. OPERATING SEQUENCES. Individual paragraphs are dedicated to each 100 Watt Transceiver mode, feature and operating sequence. A summary of the paragraphs is provided below for quick reference. These paragraphs assume the operator is familiar with the information given in section I of this chapter.

Para	Instruction
4-10.	Power Application Sequence
4-11.	Normal Positioning of Analog Controls
4-13.	Frequency Selection
4-14.	Channel Selection
4-15.	Mode Selection
4-16.	Audio Source Selection
4-17.	AGC Selection
4-18.	VOX Selection
4-19.	BFO Selection
4-20.	CLIP Selection
4-21.	Sidetone Selection
4-22.	FSK REV Selection
4-23.	TX KEY Selection
4-24.	USB and LSB Operation
4-25.	AME Operation
4-26.	CW Operation
4-27.	AFSK Operation
4-28.	Remote Operation
4-29.	Linear Power Amplifier Operation
4-30.	Antenna Coupler Operation
4-31.	Front Panel Adjustments
4-32.	BIT Fault Interpretation
4-33.	Power, VSWR, and Audio Metering
4-34.	Programming of Preset Channels

4-6. SEQUENCING OF CONTROLS. To insure that the equipment is operated properly, follow the paragraphs in the order presented. For example, Mode selection in paragraph 4-15 assumes that the Power Application Sequence has been completed in paragraph 4-10. The Front Panel Adjustments described in paragraph 4-31, and the Power, VSWR, and Audio Metering descriptions in paragraph 4-33 are general to all operations of the 100 Watt Transceiver.

4-7. CONNECTION OF EXTERNAL EQUIPMENT. The connection of external equipment is dependent on the desired configuration of the 100 Watt Transceiver. The least complicated configuration would be operation of the 100 Watt Transceiver with the supplied CW key and handset/microphone connected into a 50 ohm antenna. Other possibilities include connections to an antenna coupler, linear power amplifier, remote control, and ancillary equipment.

4-8. EXTERNAL CONNECTIONS. Most applications of the 100 Watt Transceiver have a number of external connections. Of the list below, only the first two connections are required for all applications of the equipment.

a. Power source connection

b. Antenna or antenna matrix connection

c. Linear Power Amplifier (LPA) connections

d. Antenna coupler connections

e. Audio 2 (Narrow Band Secure Voice, or similar equipment) connection

f. Telephone line connections (PATCH)

g. Teleprinter connections (when AFSK option installed)

h. Remote Control connections (when Remote option installed)

i. Audio connections to external equipment

j. Monitor connections (use RF SAMPLE (J2) and AGC (TB1) ports)

4-9. POWER APPLICATION AND WARMUP. The 100 Watt Transceiver is an all solid state equipment and requires no warmup, although up to 30 minutes may be required for stabilization of the frequency standard if it is operated after being in cold storage.. If power is connected to the 100 Watt Transceiver, and the power switch is off, the frequency standard oven is NOT powered. If the 100 Watt Transceiver is used in conjunction with a linear power amplifier, the amplifier requires a period of approximately three minutes for the filaments of the output tube to warm up. During this warm up period, the LPA is in bypass and normal 100 Watt Transceiver operation is allowed. The 100 Watt Transceiver requires 115/230 Vac or 12/28 Vdc for operation. When the 115/230 Vac or +28 Vdc power source is used, the associated Power Supply equipment is required. The procedures below assume the use of the Power Supply equipment. The power cord supplied is for ac operation only. If dc operation is desired use DC Power Cable, Harris Part Number 10085-0064. To strap the 100 watt transceiver for the desired ac or dc voltage, refer to chapter 2, paragraph 2-4.

4-10. POWER APPLICATION OPERATOR SEQUENCE. A sequence for the power application is provided below. Operations may commence before the 30-minute frequency standard stabilization period, however, transmit/receive frequency errors (less than 100 Hz) may be experienced until stabilization.

a Power Application Sequence.

(1) Turn POWER switch to ON position.

(2) Observe LCD readout contains previous frequency/mode information present at power off or default information (see paragraph 3-3).

(3) Press [2ND][REMOTE]. Observe REMOTE indicator extinguishes (if applicable).

(4) Turn on power switch for LPA and Antenna Coupler (if applicable), and select LPA AUTO and Coupler AUTO mode (for 1kW Coupler use only -AUTO control is located at the 1kW Control Unit front panel).

(5) Turn front panel speaker switch (SPKR) to ON position.

(6) Press 100 Watt Transceiver [2ND][TEST]. Observe all front panel LCD segments are turned on, followed by a readout in frequency field indicating "PASSEd". If "PASSEd" readout was not obtained, refer to paragraph 4-32 before proceeding.

(7) Allow 30 minutes for 100 Watt Transceiver frequency standard to stabilize, if required.

b. Normal settings of Audio Gain, RF Gain, and Squelch controls.

(1) Audio Gain. 1/4 turn clockwise, or adjusted to suit.

(2) RF Gain. Full clockwise position

(3) Squelch. Full counterclockwise position into OFF (detent)

4-11. ANALOG CONTROL POSITIONING.

a. Audio gain. The AUDIO GAIN control affects the front panel speaker, headset, and handset. The audio outputs available at the rear of the 100 Watt Transceiver have separate level adjustments. If the supplied headset is connected to the front panel HEADSET jack, the front panel speaker is not disconnected. Use the front panel switch if it is desired to disconnect the speaker.

b. RF gain. The RF GAIN control is typically placed in the high gain position, i.e., the knob is turned fully clockwise. In this position, the RF gain of the receiver is determined by normal AGC action. If a condition exists where normal AGC action is detrimental to reception, the RF GAIN control may be turned counterclockwise. The RF GAIN control then overrides the normal AGC circuit, and manually adjusts the gain of the receiver. Refer to paragraph 4-17 for a complete discussion of 100 Watt Transceiver AGC circuits.

c. Squelch. The SQUELCH control is usually placed into the OFF position, i.e., the knob is turned fully counterclockwise into detent. In this position, all received signals are monitored regardless of strength. If it is desired to monitor only a received signal that is strong enough to rise above the background noise, the squelch function can be enabled. If SQUELCH is desired, the correct setting of the SQUELCH control is found by turning the knob out of detent in the clockwise direction during a

period when only background noise is present in the speaker. Turn the SQUELCH control slowly clockwise until the squelch action just mutes the audio output. An incoming voice signal, above the noise level, will break the squelch and be heard in the front panel speaker. Squelch action affects the PATCH and AUD2 audio outputs as well as the front panel speaker. The LINE receive audio output is not affected by the squelch circuit. Note that the squelch responds only to voice signals and will not generally break to pass other types of signals.

4-12. CONTROL OPERATION DURING PERIODS OF TRANSMIT. Frequency and channel changes can not be made when the 100 Watt Transceiver is keyed. Only the controls [TEST],[S TONE] (there is no front panel display for Sidetone), [METER] and [CLIP] (CLIP active in voice modes only) are active when the 100 Watt Transceiver is transmitting. A keyline inhibit signal prevents equipment damage during frequency and channel changing operations.

4-13. FREQUENCY SELECTION. Minimum entry is 01.600.00 MHz, maximum entry is 29.999,99 MHz. When operating in the CW mode, an automatic 1 KHz offset is entered in transmitted frequency output. Therefore, for CW-LSB, the transmitted carrier frequency is 1 KHz below the displayed frequency; for CW-USB, the transmitted carrier frequency is 1 KHz above the displayed frequency. The select switch for CW-USB/LSB is located on the A1A2 IF Filter Assembly.

NOTE

Selection of the CW-USB/LSB switch must be made with the transceiver power turned off as the switch position is read by the internal microprocessor only when the 100 Watt Transceiver is first turned on, i.e., if the selection is made when the 100 Watt Transceiver power is on, a change in the CW-LSB/USB switch status will not be implemented.

a. Frequency Selection - Numeric Key Method.

(1) Press [FREQ] and observe word FREQ displayed in LCD frequency field.

(2) Load desired frequency into display with keypad. Following entry of each number, next digit position blinks.

(3) Press [ENTER] when frequency display is correct.

(4) Observe desired frequency is displayed in LCD frequency field, no digits are blinking, and FREQ indicator is no longer illuminated.

b. Frequency Selection - Scroll Method.

(1) Press [FREQ] and observe word FREQ displayed in LCD frequency field.

(2) Push [SCROLL UP] (also says TEST) and observe frequency changes upwards in 10 Hz steps for a short interval, and then changes to 1 KHz steps.

(3) Release [SCROLL UP]. Observe frequency display is fixed at some higher frequency. It is not necessary to use [ENTER] in this method.

(4) Push [SCROLL DOWN] (also says REMOTE) and observe frequency changes downwards in a similar manner.

(5) Release [SCROLL DOWN]. Observe frequency display is fixed at some lower frequency. It is not necessary to use [ENTER] in this method.

(6) Using [SCROLL UP][SCROLL DOWN] keys, select desired frequency.

(7) To Exit Frequency Scrolling Feature, press [ENTER].

4-14. CHANNEL SELECTION. The channel method is used when channels have been preprogrammed with operating frequency and mode (these are the only parameters that can be entered in the channel memory). When the channel feature is not used, the operating frequency and mode are entered individually, starting with the frequency.

NOTE

These instructions assume preset channels have already been programmed. If required, refer to the sequence for programming a preset channel in paragraph 4-34.

a. Channel Selection - Numeric Key Method.

(1) Press [CHAN] and observe CHAN indicator illuminates in LCD channel field.

(2) Enter the two-digit channel number into display using keypad. Minimum number is 00; maximum number is 99.

(3) Press [ENTER] when display is correct.

(4) Observe desired channel is displayed in LCD channel field and CHAN indicator is no longer illuminated.

(5) 100 Watt Transceiver will operate with frequency and mode displayed.

b. Channel Selection - Up/Down Increment Method.

(1) Press [CHAN] and observe CHAN indicator illuminates in LCD channel field.

(2) Push [SCROLL UP] (also says TEST) if desired channel is higher than number in display. Channel number now increments higher at one second intervals.

(3) Release [SCROLL UP] when desired channel is displayed. Do not use [ENTER] in this method.

4) If desired channel is lower than channel number in display, push [SCROLL DOWN] (also says (REMOTE) and observe channel number decrements at one second intervals.

(5) Release [SCROLL DOWN] when desired channel is displayed. It is not necessary to use [ENTER] in this method.

c. To Exit Channel Feature. Press [FREQ][ENTER] to exit Channel feature.

4-15. MODE SELECTION. For the USB and LSB modes, the carrier is fully suppressed. The AME mode is USB plus carrier, and the CW mode is audio derived with a plus or minus 1 KHz carrier frequency offset depending on whether CW-LSB or CW-USB has been internally selected. For AFSK mode selection, the option must be installed. Press [MODE]. Observe indicator for each mode as follows.

a. USB - Upper Sideband

b. LSB - Lower Sideband

c. AME - Amplitude Modulation Equivalent

d. CW - Continuous Wave (Morse)

e. AFSK - Audio Frequency Shift Keying (if option installed)

4-16. AUDIO SOURCE SELECTION. In the CW and AFSK modes, [AUDIO SOURCE] has no effect. AUDIO: MIC selects audio from microphone connected at front panel HANDSET/MIC jack; AUDIO: AUD2 selects audio via rear panel jack J4; AUDIO: PATCH connects a 2-wire/4-wire telephone circuit via rear panel terminal strip TB1. Press [AUDIO SOURCE]. Observe indicators below (must be a voice mode of operation):

a. AUDIO: MIC - Audio Source Microphone. The microphone audio source accepts audio and push-to-talk keyline information from the front panel HANDSET/MIC connector. A compression circuit, in series with this input, will automatically compensate for variations in input levels of ±15 dB. The compressions circuit center is set via the front panel MIC adjustment control. The input is designed to be used with a dynamic microphone and carbon type microphones may not be used.

b. AUDIO: AUD2 - Audio Source 2. The Audio 2 source accepts audio and push-to-talk keyline information from the rear panel AUD2 connector (J4). There is no compression circuit associated with the AUD2 input and it is designed to accept a 0 dBm average power speech signal from a 600 ohm source. The sensitivity of the AUD2 input is internally adjusted.

c. AUDIO: PATCH - Audio Source Telephone Patch. The PATCH source accepts audio from the rear panel PATCH terminals. There is no compression circuit associated with this input. An internal 2-wire/4-wire hybrid select switch is located on the A1A16 Audio Interface PWB and positioned as described in chapter 2, paragraph 2-3. The 2 or 4 wire telephone circuits permit direct telephone-to-radio communication. The phone patch permits phone line audio to be coupled to the transceiver

transmit circuitry and transceiver receive audio to be coupled to the connected telephone line.

CAUTION

After completing a phone PATCH, or prior to receipt of an incoming call, assure the Transceiver Audio Source is set to the MIC or LINE Setting. Damage may occur to the Transceiver by the phone line ring voltage if the PATCH is enabled when the phone ring circuits are activated.

NOTE

When connecting to the telephone network, a data or voice coupler unit approved by the applicable regulatory agency (the Federal Communications Commission in the United States) should be used.

Both the incoming and outgoing phone patch audio levels are metered and adjustable via the front panel controls (see paragraph 4-31). Selection of two or four wire operation is made via a switch located on the Audio Interface PWB, A1A16 (see figure 1-3 for location). To access this switch, remove the top cover of the transceiver, and locate the switch by the assembly. Receive audio will only be present at the PATCH terminals when PATCH is selected as an audio source. The phone patch can accept and can supply audio signal levels from less than -20 dBm to 0 dBm, as adjusted at the recessed front panel controls.

4-17. AGC SELECTION.

a. AGC OFF Mode. The AGC: OFF mode is used when the gain of the receiver is to be under total manual control with the front panel RF GAIN adjustment. To select the AGC: OFF mode, press [2ND][AGC OFF]. Observe AGC Indicators:

AGC: OFF (AGC: OFF selected)

NOTE

When going from AGC: OFF to AGC enable, the previously selected AGC speed will be reestablished.

b. AGC Speed Selection. The AGC characteristic is fast attack and slow decay. The attack time is constant at 30 milliseconds, and decay time is variable at SLOW, MED, or FAST. When a mode of operation (USB, LSB, AME, CW or AFSK) is selected, an AGC speed is automatically selected typical for operations in that mode. For example, in SSB voice operations, the AGC: SLOW speed is desired since pauses in speech patterns represent no input signal, and with a slow AGC decay, the AGC is held steady preventing an increase in background noise. To select AGC speed, press [AGC]. Observe indicators.

(1) AGC: SLOW (3± 1 second)

(2) AGC: MED (200 ± 100 milliseconds)

(3) AGC: FAST (30 milliseconds or less)

NOTE

[AGC] has no effect if the AGC indicator reads AGC: OFF.

4-18. VOX SELECTION. The VOX (Voice Operated Transmit) feature is used to automatically generate a keyline when transmit audio is detected. There is a choice of two VOX decay time constants; a long decay for voice signals, and a short decay for data signals. These determine the amount of time that will elapse following a pause in the transmit audio before the tranceiver switches back to receive. The voice time constant is internally adjustable. There are two front panel adjustments for the VOX circuit, the VOX and the ANTIVOX. The VOX adjustment sets the threshold level required to trigger the VOX circuit. The ANTIVOX circuit samples the received speaker audio and counteracts the effect of the microphone picking up the receive audio signal, thereby preventing false VOX operation. ANTIVOX

is adjusted for the acoustical coupling between speaker and microphone, and should be adjusted only when the microphone is in a fixed position. The adjustment procedures for the front panel VOX and ANTIVOX controls are discussed in paragraph 4-31. The VOX feature is selected by pressing [2ND][VOX]. Observe indicators.

a. VOX VOICE

b. VOX DATA

c. VOX OFF (no VOX indicator)

4-19. BFO SELECTION. The BFO is used to raise or lower the pitch of received audio signals in all modes except AME. The Beat Frequency Oscillator (BFO) feature is selected by pressing [BFO]. The BFO indicator will illuminate. Use the [SCROLL UP]/ [SCROLL DOWN] keys to adjust the BFO in 10 Hz steps over a ± 1 kHz range. Each keystroke enters a 10 Hz step, or hold down the scroll keys for continuous entry. The BFO ON ± indicator will illuminate to indicate the position of the BFO relative to center when the BFO is off-center. There is no frequency read-out of the BFO offset. Remember the following BFO characteristics:

a. The BFO function will not change the pitch of the received audio signals when operating in the AME mode.

b. The maximum BFO offset is ±1000 Hz.

c. There is no display for the BFO frequency. Instead, there is a "BFO ON (+)" indication or "BFO ON (-)" indication. If the BFO is at center frequency, the "BFO ON" indicator is not illuminated.

d. BFO offset is entered with scroll keys with a change of 10 Hz per keystroke. Count keystrokes for desired offset.

4-20. CLIP SELECTION. The CLIP function is selectable only in voice modes from the MIC and PATCH sources. The feature is used for peak clipping of the transmit audio levels to increase the average RF output levels. The clipper is adjustable internally from 0 dB to 12 dB. The CLIP function is selected by pressing [2ND][CLIP]. Observe indicator CLIP illuminates when clipping feature is selected.

4-21. SIDETONE SELECTION. The sidetone feature is used to inject a portion of the transmit audio into the receive audio path. This is useful for the operator in voice modes for headset feedback, in CW mode for a 1 KHz tone when the CW key is closed, or to monitor the transmit audio during any mode of operation. The sidetone (S TONE) function is selected by pressing [2ND][S TONE]. There is no indicator for sidetone function, and sidetone is automatically selected when operating in the CW mode.

4-22. FSK REV SELECTION. The FSK REV function is selectable only in the AFSK mode. The feature is used to reverse the sense of the AFSK Keyer (KREV), the AFSK Converter (CREV), or both. The FSK REV function is selected by pressing [2ND][FSK REV]. Observe indicators (there is no indicator for Normal sense).

a. Normal/KREV

b. CREV/Normal

c. CREV/KREV

d. Normal/Normal

4-23. TX KEY SELECTION. The TX KEY function is selectable in all modes of operation. The feature may be used to generate a keyline whenever the normal keyline is absent, to enable transmit BIT, for test procedures, etc. The TX KEY function is selected by pressing [2ND][TX KEY]. Observe indicator XMIT illuminates when transmitter is keyed. In the CW mode, a CW key closure is also required to obtain output power.

4-24. USB AND LSB OPERATION. The single sideband modes, Upper Sideband (USB) and Lower Sideband (LSB), operate with a suppressed carrier. The bandwidth of the SSB filters is 350 Hz to 3050 Hz. The procedures to operate in the USB or LSB modes, including all features available to the operator, are found in the following references.

a. Perform Power Application Sequence, paragraph 4-10.

b. Perform Analog Control Positioning, paragraph 4-11.

c. Perform Channel Selection, paragraph 4-14, if preprogrammed.

d. Perform Frequency Selection, paragraph 4-13.

e. Perform Mode Selection, paragraph 4-15, selecting USB or LSB.

f. Perform Audio Source Selection, paragraph 4-16.

g. Perform AGC Selection, paragraph 4-17, default is AGC: SLOW.

h. Perform VOX Selection, paragraph 4-18.

i. Perform BFO Selection, paragraph 4-19.

j. Perform CLIP Selection, paragraph 4-20.

k. Perform Sidetone Selection, paragraph 4-21.

l. Perform Linear Power Amplifier Selection, paragraph 4-29.

m. Perform Antenna Coupler Sequence, paragraph 4-30.

n. Reference Front Panel Adjustments, paragraph 4-31.

o. Reference Power, VSWR, and Audio Metering, paragraph 4-33.

p. Use local or remote keyline to transmit.

4-25. AME OPERATION. The AME (Amplitude Modulation Equivalent) operates with carrier and upper sideband. The carrier is normally 25 watts but the PEP resulting when modulated is a full 100 watts. The IF filter for the AME mode is the same filter used in the USB mode, with a 3 dB bandwidth of 350 Hz - 3050 Hz. AME is also known as compatible AM. The procedure to operate in the AME is found in the following references.

a. Perform Power Application Sequence, paragraph 4-10.

b. Perform Analog Control Positioning, paragraph 4-11.

c. Perform Channel Selection, paragraph 4-14, if preprogrammed.

d. Perform Frequency Selection, paragraph 4-13.

e. Perform Mode Selection, paragraph 4-15, selecting AME.

f. Perform Audio Source Selection, paragraph 4-16.

g. Perform AGC Selection, paragraph 4-17, default is AGC: FAST.

h. Perform VOX Selection, paragraph 4-18.

i. Perform Sidetone Selection, paragraph 4-21.

j. Perform Linear Power Amplifier Selection, paragraph 4-29.

k. Perform Antenna Coupler Sequence, paragraph 4-30.

l. Reference Front Panel Adjustments, paragraph 4-31.

m. Reference Power, VSWR, and Audio Metering, paragraph 4-33.

n. Use local or remote keyline to transmit.

4-26. CW OPERATION. The CW mode (Morse) is full carrier transmission without modulation. A frequency offset of exactly 1 KHz will automatically occur resulting in transmissions 1 KHz above (CW-USB) or 1 KHz below (CW-LSB) the displayed frequency. The switch for the CW Sideband Select is located on the A1A2 IF Filter PWB the positioning of which is described in chapter 2, paragraph 2-4. The 3 dB bandwidth of the CW filter is ±200 Hz centered at 455 KHz. If the recovered 1 KHz tone is to be raised or lowered, the BFO feature may be used. An internally adjustable CW hang-time is provided that determines the amount of time that elapses following the last transmitted CW character before the transceiver switches to the receive mode. Note that in the CW mode, the entry [2ND][TX KEY] will not cause power to be transmitted. When the [2ND][TX KEY] is used, it places the transmitter into a transmit configuration but the CW key must be closed to obtain power out. The procedures to operate in the CW mode are found in the following references.

a. Perform Power Application Sequence, paragraph 4-10.

b. Perform Analog Control Positioning, paragraph 4-11.

c. Perform Channel Selection, paragraph 4-14, if preprogrammed.

d. Perform Frequency Selection, paragraph 4-13.

e. Perform Mode Selection, paragraph 4-15, selecting CW.

f. Perform AGC Selection, paragraph 4-17, default is AGC: SLOW.

g. Perform BFO Selection, paragraph 4-19.

h. Perform Sidetone Selection, paragraph 4-21.

i. Perform Linear Power Amplifier Selection, paragraph 4-29.

j. Perform Antenna Coupler Sequence, paragraph 4-30.

k. Reference Front Panel Adjustments, paragraph 4-31.

l. Reference Power, VSWR, and Audio Metering, paragraph 4-33.

m. Use CW keyline to transmit.

4-27. AFSK OPERATION. It is important that the AFSK equipment at each end of the radio link be adjusted for the same sideband, center frequency, and frequency shift. The AFSK option has the following capabilities; a 850 Hz shift with a center frequency of 2000 Hz, a 170 Hz shift with a center frequency of 2000 Hz, or a 85 Hz shift with a center frequency of 2805 Hz and LSB or USB sideband selection. Shift and sideband selection is made at theAFSK configuration switch located on the AFSK IF Filter PWB, A1A18A2. To select the desired AFSK switch position, refer to chapter 2, paragraph 2-4.

a. AFSK Tuning. An indication of the correct tuning of an AFSK received signal may be obtained by using the AFSK Meter function. When receiving a correctly tuned AFSK transmission (not a steady Mark or Space, however) the AFSK meter segment should be positioned over the central arrow shown on the meter scale. If this is not the case, the operating frequency of the 100 Watt Transceiver may be changed using the scroll keys until the correct center indication is obtained.

b. Mark Hold. If sufficient received signal is not present at the input of the AFSK module for reliable error free operation, the unit will force a mark-hold condition to the teleprinter. Under certain circumstances, high received noise levels may cause the mark hold to be released and the teleprinter to print randomly. This can be stopped by reducing the RF GAIN control on the front panel until the teleprinter is forced back to a mark-hold condition.

c. AFSK Normal and Reverse Keyer/Converter Sense. The normal sense is consistent with MIL-STD-188-114 where (+) = binary 0 = space, and (-) = binary 1 = mark. If KREV (Keyer Reverse for transmit) or CREV (Converter Reverse for receive) is selected, the respective sense is reversed with (+) = binary 1 = mark, and (-) = binary 0 = space.

d. AFSK Frequency Compensation. It is possible to compensate at the 100 Watt Transceiver for other AFSK center frequencies. This is accomplished by adjusting the operating frequency of the 100 Watt Transceiver by the amount of the difference. The procedure uses the AFSK Relative Center Frequency meter scale where the distant party transmits a series of "RY" characters (for example) and the receiving party observes the AFSK meter. The frequency of the 100 Watt Transceiver is then adjusted (+) or (-) to zero out any offset.

e. AFSK Operation Sequence.

(1) Perform Power Application Sequence, paragraph 4-10.

(2) Perform Analog Control Positioning, paragraph 4-11.

(3) Perform Channel Selection, paragraph 4-14, if preprogrammed.

(4) Perform Frequency Selection, paragraph 4-13.

(5) Perform Mode Selection, paragraph 4-15, selecting AFSK.

(6) Perform AGC Selection, paragraph 4-17, AGC: MED.

(7) Perform BFO Selection, paragraph 4-19.

(8) Perform Sidetone Selection, paragraph 4-21.

(9) Perform FSK Reverse Selection, paragraph 4-22.

(10) Perform Linear Power Amplifier Selection, paragraph 4-29.

(11) Perform Antenna Coupler Sequence, paragraph 4-30.

(12) Reference Front Panel Adjustments, paragraph 4-31.

(13) Reference Power, VSWR, and Audio Metering, paragraph 4-33.

(14) Use local or remote keyline to transmit.

4-28. REMOTE OPERATION. The transceiver can be operated in remote control in any mode except AFSK. When the remote control mode is selected, all 100 Watt Transceiver keys are disabled except [2ND]/[REMOTE]. The local RF GAIN control is also disabled while in remote mode. If the 100 Watt Transceiver loses communications with the Remote

Control, the 100 Watt Transceiver enters an Idle Mode where the LPA (if any) is turned off, the display indicates "rcu OFF," and the 100 Watt Transceiver is in the receive mode with muted audio output. Since the 100 Watt Transceiver is still in the remote mode, the front panel keys and controls are disabled. For additional information for operating in the remote control mode, refer to the Remote Control manual. When the remote option is installed, press [2ND][REMOTE] to toggle between local and remote control operation. Observe indicator REMOTE illuminates when remote mode is selected.

4-29. LINEAR POWER AMPLIFIER OPERATION. The 100 Watt Transceiver may be operated with a 500 Watt or 1000 Watt Linear Power Amplifier (LPA). Complete instructions for LPA operation will be found in the associated LPA manuals. The antenna coupler tuning sequence is automatically integrated with the LPA tuning sequence. If the LPA has been previously tuned at the operating frequency, going from AMP: STBY to AMP: OPER will not initiate another LPA tune cycle. A new LPA tune sequence is initiated when the operating frequency is changed by more than 1%. If the AUTO mode is selected at the LPA, the sequence for placing the LPA into service is as follows.

a. Complete all sequences for features and operating parameters as discussed in preceding paragraphs.

b. Press [2ND][AMP PWR]. Observe indicator AMP: STBY illuminates with the STBY portion flashing.

c. Wait a nominal 3 minutes and observe STBY indicator portion stops flashing. (Waiting period allows LPA final amplifier tube filaments to warm up.)

d. Press [2ND][STB/OPR]. Observe indicator now reads, AMP: OPER with the OPER portion flashing (indicating the LPA requires a tune sequence).

e. To initiate an LPA tune sequence, momentarily close the keyline associated with mode of operation, or use the TX KEY sequence discussed in paragraph 4-23. Observe indicator OPER stops flashing when LPA is tuned.

NOTE

This step automatically initiates tune sequence for a companion Antenna Coupler, if used (see paragraph 4-30). When the antenna coupler is tuning, the indicator TUNE illuminates.

f. Remove keyline used to initiate LPA tune cycle; LPA is now ready for normal operations.

g. To place LPA in standby mode, unkey the 100 Watt Transceiver, and press [2ND][STB/OPR]. Observe LPA indicator AMP: STBY illuminates. The LPA is now bypassed and the 100 Watt Transceiver operates directly into the associated antenna coupler.

NOTE

If 100 Watt Transceiver is keyed, [STB]/[OPR] will have no effect.

h. To deenergize the LPA, press [2ND][AMP PWR]. Observe indicator AMP:STBY is no longer illuminated and LPA is shut down.

4-30. ANTENNA COUPLER OPERATION. There are no direct controls for the 100/500 Watt Antenna Coupler, but there is a control unit associated with the 1000 Watt Antenna Coupler. Operation of the 100/500 Watt Antenna Coupler or operation of the 1000 Watt Antenna Coupler (if placed in AUTO) is completely automatic and requires no special operating sequence. During an antenna coupler tune sequence, the front panel TUNE indicator illuminates. If the antenna coupler was unable to tune, the indicator BYPASS illuminates. BYPASS indicates that the antenna coupler is bypassed and the antenna is connected directly to the 100 Watt Transceiver/LPA. The 100 Watt Transceiver will transmit when the antenna coupler is bypassed, and automatically reduce transceiver output power to accommodate any encountered VSWR. During the tune sequence for the antenna coupler, a much lower RF level is used for tuning. This may cause indicator LO PWR to illuminate, which is a normal occurrence. When the antenna coupler is tuned, full power is applied and a LO PWR indication would reflect a genuine low power condition.

4-31. FRONT PANEL ADJUSTMENTS. There are six maintenance controls available to the operator. Each control and its adjustment procedure is discussed below.

a. VOX Adjustments. The VOX feature has two maintenance controls; the VOX threshold and the ANTIVOX threshold. The VOX threshold sets the threshold for the audio level required to trigger the transmitter keyline, and the ANTIVOX sets the threshold for prevention of a keyline during periods of reception.

(1) VOX Threshold Procedure

(a) Connect a microphone to the front panel jack.

(b) Select the VOX feature using the procedure in paragraph 4-18.

(c) Speak normally into the microphone and adjust the front panel VOX adjustment clockwise until the transmitter goes into the transmit mode.

(d) Stop speaking into the microphone and observe the transmitter unkeys.

(2) ANTIVOX Threshold Procedure

(a) Tune in a typical radio transmission and adjust the speaker volume for normal listening level.

(b) Select the VOX feature using the procedure in paragraph 4-18.

(c) Connect a microphone to the front panel jack.

(d) Do not speak into the microphone, and adjust the ANTIVOX control counterclockwise until the transmitter keys. When this happens, turn the ANTIVOX control clockwise until the transmitter unkeys. If significant speaker-to-microphone coupling is not present, the transmitter will not key and the Antivox may be left at minimum.

NOTE

There is interaction between the VOX and ANTIVOX adjustments. It may be necessary to conduct these procedures twice, or more, to suit your operational conditions. Be careful not to transmit during another station's transmissions or on unauthorized frequencies.

b. PATCH Adjustments. The PATCH RCV and PATCH XMIT maintenance controls are used to set the levels to and from the 2-wire/4-wire external telephone patch connections, respectively. These controls are set when the audio source is PATCH as follows:

(1) PHONE XMIT Procedure

(a) Establish a phone patch circuit.

(b) Select the front panel meter function AUDIO as described in paragraph 4-33.

(c) Observe the audio peaks on the meter and set the PATCH TX control for voice peaks at 0 dB.

(d) Continue directly to PHONE RCV procedure below.

(2) PHONE RCV Procedure

(a) Select the front panel meter function PATCH as described in paragraph 4-33.

(b) Observe the level of the voice peaks present during normal received conversation.

(c) Adjust the PHONE RCV such that the voice peaks observed in (b) above are -10 dBm. This level may be adjusted upwards if the phone user reports weak received audio.

c. MIC Adjustments. The MIC maintenance control is active when the audio source is MIC. The MIC control adjusts the input transmit audio levels as follows:

(1) Connect a front panel microphone to the equipment.

(2) Select the front panel meter function AUDIO using the procedure in paragraph 4-33.

(3) Press the PTT microphone button and talk normally into the microphone. Observe the audio peaks on the front panel meter.

(4) Adjust the MIC control such that voice peaks register "0" (0 dB) on the meter display.

(5) Unkey the transmitter. This completes the procedure. Note that increasing the level above the 0 dB point will not increase RF power but will only cause excessive noise to be transmitted during speech pauses.

d. LINE Adjustments.

(1) Connect the desired termination to the LINE output terminals at the rear of the equipment via TB1.

(2) Select the front panel meter function LINE using the procedure in paragraph 4-33.

(3) Tune in a radio transmission typical for operations and observe the audio peaks on the front panel meter. A steady tone provides the best results.

(4) Adjust the LINE control for the desired level (between -20 dBm to +10 dBm).

4-32. BIT FAULT INTERPRETATION. The 100 Watt Transceiver has the capability to troubleshoot itself and give an indication of any failure or reduced performance condition. During transmitter BIT testing, full RF power is generated and appears at the rear panel RF INPUT/OUTPUT jack J1. (The transmitted frequency is the frequency entered prior to BIT testing.) To prevent accidental transmissions, or create a hazardous situation, the 100 Watt Transceiver must be keyed and tuned to initiate the transmit BIT test sequence. If the 100 Watt Transceiver is not keyed when BIT is selected, only the receiver portion of the 100 Watt Transceiver is tested. If the 100 Watt Transceiver is keyed when BIT is selected, both the receiver and transmitter portions of the 100 Watt Transceiver are tested. Detailed discussions of the BIT fault codes are in chapter 6.

a. BIT Feature Sequence - Receiver Only. Press [2ND][TEST] and observe all indicators illuminate during test, followed by the word "PASSEd" in frequency display.

b. BIT Feature Sequence - Receiver and Transmitter. Press [2ND][TX KEY][2ND][TEST]. Observe all indicators illuminate during test, followed by the word "PASSEd" in frequency display. Press [2ND][TX KEY] After "PASSEd" extinguishes.

CAUTION

Verify the RF OUTPUT jack, J1, is terminated into a 100 watt dummy load, or suitable antenna when BIT testing includes the transmitter. If a 500 Watt or 1 KW linear Power Amplifier is connected in the system, verify that its output jack (J5) is terminated into the dummy load or antenna. Be careful not to transmit on unauthorized frequencies or interfere with other transmissions.

c. BIT Fault Codes. If a BIT test has detected a fault, an indication of the difficulty will be displayed in the front panel frequency LCD. The faults are coded as listed below (see Chapter 6 for further BIT information).

Display Fault

1 A1A1 EXCITER

-0 No Exciter Module installed
-1 No 455 KHz modulator output
-3 No 40 MHz modulator USB output
-4 No 40 MHz AME modulator output
-5 No 40 MHz modulator CW output

1 A1A2 IF FILTER

-1 No USB IF
-2 No LSB IF
-3 No CW IF

1 A1A3 FIRST CONVERTER

-1 No 1st Converter receive output
-2 No 1st Converter transmit output

1 A1A4 100 WATT PA

-1 No PA output

1 A1A5 LOWPASS FILTER

Display	Fault
-1	LPF band 1 open (receive)
-2	LPF band 2 open (receive)
-3	LPF band 3 open (receive)
-4	LPF band 4 open (receive)
-5	LPF band 5 open (receive)
-6	LPF band 6 open (receive)
-7	LPF latched closed (receive)
-8	VSWR fault (transmit)
-9	LPF open (transmit)

1 A1A6 AGC/TGC

-1	AGC high
-2	No manual RF Gain Control
-3	TGC Set Point is incorrect
-4	No TGC action

1 A1A7 RECEIVER

-0	No Receiver Module installed
-1	No 2nd Converter receive signal
-2	Low Receive Line Level
-3	Bad Receiver T/R switch (no transmit signal)
-4	AGC Set Point is incorrect

1 A1A9 REF/BFO

-1	BFO unlock

1 A1A10 SYNTHESIZER

-0	No Synthesizer Module installed
-1	Synthesizer unlocked

1 A1A12 CONTROL

-1	Analog/Digital Converter defective

1 A1A13 LPA/COUPLER INTERFACE

-0	No LPA/Coupler Interface Module installed

1 A1A14 MULTIVOLTAGE CONVERTER

-1	High voltage
-2	Low voltage

1 A1A18 AFSK

-1	No AFSK output

Display	Fault
-2	No AFSK IF present

1 A1A19 REMOTE INTERFACE

-1	Invalid baud rate
-2	UART loopback fault

NOTE

If A1A19 Fault is indicated, ensure that the Remote Control Unit is turned on, and repeat the BIT test prior to replacement.

2 LINEAR POWER AMPLIFIER (LPA)

-00	No LPA test set by Transceiver
-01	Micro-control fault
-02	Not used
-03	Primary power fault
-04	+13.6V supply fault
-05	Transmitter fault
-06	Bandswitch drive fault
-07	Servo coil drive fault
-08	High voltage on in Standby
-09	High voltage fault in Operate
-10	Plate current on with bias off
-11	Plate current fault with bias on
-12	RF mute not working
-13	No RF input with Tune Power Request
-14	Plate current fault when keyed
-15	No tune peak with RF input power
-16	Forward power fault
-17	VSWR/Reflected power fault
-18	Power gain fault
-19	(Not used)
-20	Auto tune fault (not a BIT code)
-21	LPA-Transceiver link fault (not a BIT code)
-22	Plate current without forward power (not a BIT code)

3 COUPLER

-01	Coupler fault (not a BIT code)
-02	Overtemperature fault (not a BIT code)

4 REMOTE

-01	Audio Loopback Fault
-02	Invalid Baud Rate

4-33. POWER, VSWR, AND AUDIO METERING. The 100 Watt Transceiver metering feature provides for measurement of audio levels, signal strength, power, and VSWR. Selection of each meter feature is discussed below.

a. Metering Feature Selection. Press [METER]. Observe key scrolls meter through the following functions and scales.

(1) "S" Scale. Received signal strength. Scale from S3 to +60dB. This scale is automatically selected when in the receive mode and meter is set to FWD, REF, or VSWR.

(2) AUDIO. Transmit audio signal strength. Scale from -20 dB to +10 dB. Correct level is 0 dB.

(3) LINE. Receive Line audio signal. Remote line input signal when keyed. Scale from -20 dBm to +10 dBm.

(4) PATCH. Patch input signal (TX) or Patch output signal (RX). Patch input signal when keyed. Scale from -20 dBm to +10 dBm.

(5) FWD.

TX - Forward power output. Scale from 0 watt to 150 watts. With 500 Watt LPA or 1000 watt LPA, scale is WATTS X 10 (0 watt-1500 watts).

RX - Received signal strength. Scale from S3 to +60dB.

[6] REF.

TX - Reflected power. Scale from 0 watt to 150 watts. With 500 Watt LPA or 1000 watt LPA, scale is WATTS X 10 (0 watt-1500 watts).

RX - (Same as FWD.)

(7) VSWR.

TX - Voltage Standing Wave Ratio. Scale from 1 (1:1) to 4 (4:1).

RX - (Same as FWD.)

(8) AFSK. Audio Frequency Shift Keying. Shows relative center frequency with arrow indicating midscale and bar indicator offset left (-) or right (+).

NOTE

This meter reading is correct only when the average mark and space signals of the incoming signal are equal. Use a series of "RY" characters if possible - a steady mark or space will not yield an accurate meter reading.

4-34. PROGRAMMING OF PRESET CHANNELS. When using the procedure below, any previous programming of a channel will be displayed. The new information is entered, displacing the previous programming. Only frequency and mode information can be stored in the channel memory. The remainder of the features must be entered manually or the default characteristic will govern, i.e., selecting mode USB automatically selects an AGC speed of AGC: SLOW - if AGC: FAST is desired, this must be entered manually after the channel is selected. After a channel is programmed, the 100 Watt Transceiver will display the operating conditions that were set before programming started. The 100 Watt Transceiver has the capability of storing the operating parameters frequency and mode for 100 channels (00 through 99). The procedure to place this information into memory is described below:

a. Press [2ND][PROG]. Observe CHAN indicator illuminates.

b. Enter a channel number 00 to 99 with keypad, then press [ENTER]. Observe FREQ indicator illuminates.

c. Enter a frequency 01,600.00 to 29,999.99 with keypad. When frequency is correct, continue to step d.

d. Press [MODE] until desired operating mode is displayed. When mode is correct, continue to step e.

e. Observe desired frequency and mode information is entered correctly; press [2ND][LOAD].

f. This completes programming of a preset channel. Repeat procedure for each channel to be programmed.

Section III. EMERGENCY OPERATION

4-35. CONDITIONS FOR EMERGENCY OPERATION. Under certain emergency conditions, the Remote Control may still be functional with the 100 Watt Transceiver either at full performance or reduced performance depending on the fault. The procedure below details the sequence for emergency operation of the 100 Watt Transceiver from the Remote Control.

a. Difficulty - Ancillary Equipment Failure:

(1) Resolution - Disconnect the ancillary equipment, although for most failures, ancillary equipment automatically goes into a bypass mode and disconnection may not be necessary.

(2) If the 100 Watt Transceiver is used with a 500 Watt LPA and the LPA fails, the LPA will automatically go into a bypass mode. The bypass mode means the input RF power is routed straight through the LPA from input to output. The system will continue to operate normally, with 100 watt transmitter power.

(3) One possible indication of a LPA failure is the illumination of the 100 Watt Transceiver FAULT lamp and the indicator AMP:STBY.

NOTE

Paragraphs (4) and (5) apply to the 100/500 Watt Antenna Coupler only. The 1000 Watt Antenna Coupler, AN/URA-38( ), does not bypass.

(4) If an antenna coupler has failed, the 100 Watt Transceiver is connected directly to the antenna as indicated by the BYPASS indicator. The BYPASS readout means the antenna coupler is unable to tune and has been bypassed. The bypass circuit can handle full RF output levels. In antenna coupler bypass, much of the power applied to the antenna will be reflected due to the impedance mismatch, and the 100 Watt Transceiver or LPA will reduce its output power level for equipment self-protection.

(5) If the failure is not in the antenna coupler, there still may be a BYPASS indication. In this instance, the actual failure (open antenna cable, damaged antenna, etc.) would have to be determined and appropriate action taken.

b. Difficulty - Failure within the 100 Watt Transceiver.

(1) Resolution - Analyze failure and alternatives.

(2) Virtually all 100 Watt Transceiver failures will result in a FAULT indication at the Remote Control front panel. The Built In Test (BIT) feature will identify which fault has occurred as discussed in paragraph 4-32.

CHAPTER 5

THEORY OF OPERATION

Section I. FUNCTIONAL SYSTEM OPERATION

WARNING

Dangerous voltages exist in this radio equipment. Before removing any cover, disconnect primary power.

5-1. TRANSCEIVER FUNCTIONAL OPERATION. Section I provides an overall functional description of the transceiver at the major component level. Detailed descriptions of transceiver modules and assemblies are provided in section II of this chapter. Refer to FO-13 for the following brief transceiver technical description.

5-2. TRANSCEIVER OPERATING AS A RECEIVER. When the transceiver is operating as a receiver, an input signal at the antenna between 1.6 and 30 MHz passes through the low pass filter and the T/R (Transmit/Receive) switch to the first conversion mixer. The mixer converts the input signal into a 40.455 MHz intermediate frequency which is bandpass filtered, amplified, and leveled by an AGC circuit. The 40.455 MHz IF signal is applied to a second mixer and converted into an IF frequency of 455 KHz which is amplified, bandpass filtered, leveled by additional AGC circuits and applied to the demodulation circuits. For all modes of operation except AME, the signal is demodulated by a product detector (the AME mode uses an envelope detector). The resultant audio is applied to a front panel speaker and routed to rear panel terminals for external equipment.

5-3. TRANSCEIVER OPERATING AS A TRANSMITTER. When the transceiver is operating as a transmitter, the input audio is amplified and applied to a modulator for conversion into an IF frequency of 455 KHz . The 455 KHz IF signal is amplified, bandpass filtered, leveled by an ALC circuit and converted to 40.455 MHz. The 40.455 MHz IF is amplified, filtered and converted to the transmit frequency. The transmit frequency is leveled by a Transmitter Gain Control (TGC) circuit, then raised by power amplifiers to the 100 watt RF output level. The output RF is routed via a T/R switch to the lowpass filters and directional coupler. The directional coupler provides forward and reflected power measurement outputs used for front panel displays and for power control.

5-4. FUNCTIONAL OPERATION AND SIGNAL FLOW OF TRANSMITTING CIRCUITS. For the following discussion of the transmitting circuits, refer to figure FO-1.

a. Transmit Audio Selection. The transmit audio is primarily selected by the front panel AUDIO SOURCE key from one of three sources: MIC audio from a front panel handset/mic, AUDIO 2 audio from an external equipment, or PATCH audio from a 2-wire or 4-wire telephone-type circuit. Rear terminal connections are used for AUDIO 2 and PATCH audio inputs. If the transceiver is operated in the AFSK mode, the microprocessor automatically selects the AFSK audio source, which is not a function of the AUDIO SOURCE key, and all other audio sources are disconnected. A 1 KHz audio signal is automatically injected during audio derived CW transmissions, and the BIT self-test sequence. A rear panel LINE input is provided for remote operation.

b. Transmit Audio Level Adjustments. Level adjustments are provided for each of the input audio sources. For a handset/mic connection, the front panel MIC adjustment is used. For a telephone patch connection, the front panel PATCH XMIT adjustment is used. The LINE IN and AUDIO 2 audio lines have internal potentiometers, since the external equipment controls are typically used to set the input level. Each audio source has a stage of amplification or buffering except for AFSK and BIT audio.

c. Transmit Audio Compressor. The selected audio input is sampled by the front panel metering circuit and VOX circuit, and applied to a compressor circuit. The compressor circuit is not under operator control but is automatically enabled ONLY when the MIC audio source is selected. For all other audio sources, the compressor circuit is bypassed. The purpose of the compressor circuit is to equalize varying voice levels so that the audio signal is more uniform in amplitude. The circuit is used only in the

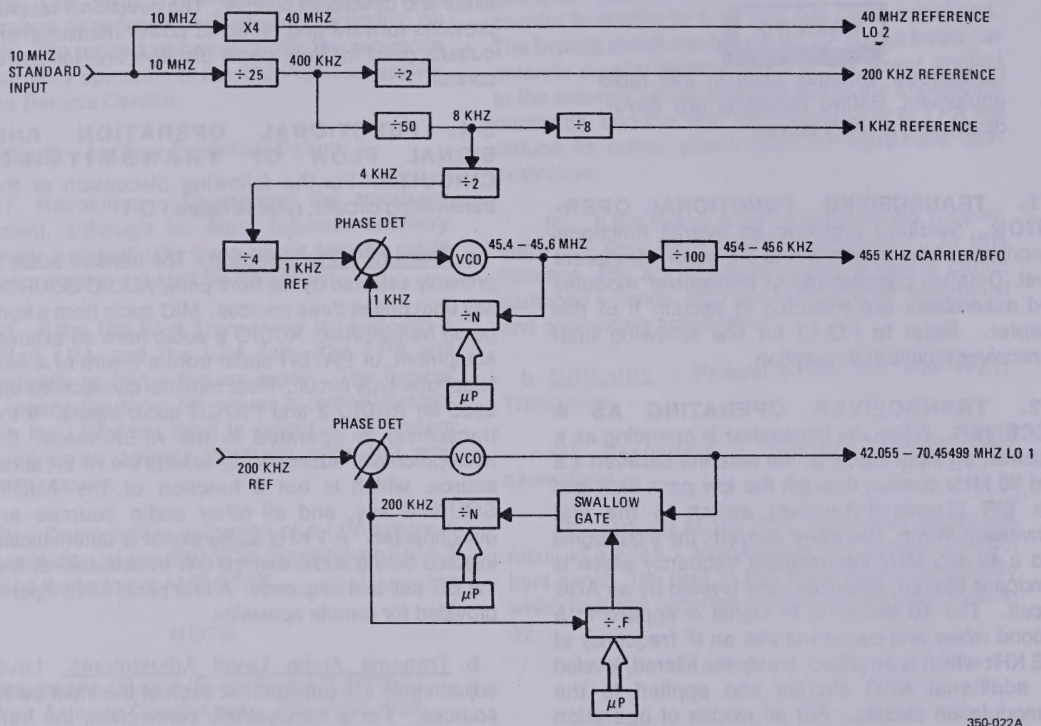
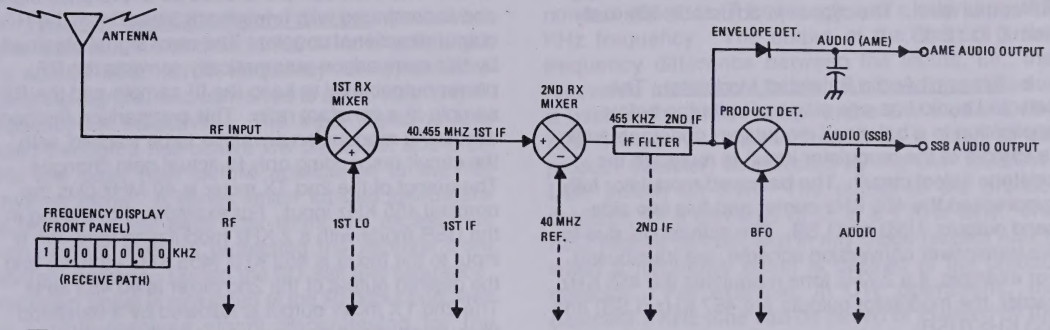


Figure 5-1 . Transceiver Reference and Synthesizer Frequencies (Sheet 1 of 2)



USB (1 KHZ TONE)	10.001,000 MHZ	50.455 MHZ	40.454 MHZ	40.000 MHZ	454 KHZ	455 KHZ	1 KHZ
LSB (1 KHZ TONE)	9,999,000 MHZ	50.455 MHZ	40.456 MHZ	40.000 MHZ	456 KHZ	455 KHZ	1 KHZ
CW (USB)	10.001,000 MHZ	50.456 MHZ	40.455 MHZ	40.000 MHZ	455 KHZ	456 KHZ	1 KHZ
CW (LSB)	9,999,000 MHZ	50.454 MHZ	40.455 MHZ	40.000 MHZ	455 KHZ	454 KHZ	1 KHZ
AME	10.000,000 MHZ(C) 10.001,000 MHZ(SB)	50.4546 MHZ 50.4546 MHZ	40.4546 MHZ 40.4536 MHZ	40.000 MHZ 40.000 MHZ	454.6 KHZ 453.6 KHZ	---- ----	1 KHZ
AFSK - 85 HZ SHIFT (USB) 2,805 HZ CTR.	10,002,847.5 HZ(S) 10,002,762.5 HZ(M)	50.457,805 MHZ 50.457,805 MHZ	40,454,957.5 HZ 40,455,042.5 HZ	40.000 MHZ 40.000 MHZ	454,957.5 HZ 455,042.5 HZ	455.5 KHZ 455.5 KHZ	542.5 HZ (SPACE) 457.5 HZ (MARK)
AFSK - 85 HZ SHIFT (LSB) 2,805 HZ CTR.	9,997,152.5 HZ(S) 9,997,237.5 HZ(M)	50.452,195 MHZ 50.452,195 MHZ	40,455,042.5 HZ 40,454,957.5 HZ	40.000 MHZ 40.000 MHZ	455,042.5 HZ 454,957.5 HZ	454.5 KHZ 454.5 KHZ	542.5 HZ (SPACE) 457.5 HZ (MARK)
AFSK - 170 HZ SHIFT (USB) 2,000 HZ CTR.	10.002,085 MHZ(S) 10.001, 915 MHZ(M)	50.457 MHZ 50.457 MHZ	40,454,915 MHZ 40,455,085 MHZ	40.000 MHZ 40.000 MHZ	454,915 KHZ 455,085 KHZ	456 KHZ 456 KHZ	1,085 HZ (SPACE) 915 HZ (MARK)
AFSK - 170 HZ SHIFT (LSB) 2,000 HZ CTR.	9.997,915 MHZ(S) 9.998,085 MHZ(M)	50.453 MHZ 50.453 MHZ	40,455,085 MHZ 40,454,915 MHZ	40.000 MHZ 40.000 MHZ	455,085 KHZ 454,915 KHZ	454 KHZ 454 KHZ	1,085 HZ (SPACE) 915 HZ (MARK)
AFSK - 850 HZ SHIFT (USB) 2,000 HZ CTR.	10.002,425 MHZ(S) 10.001,575 MHZ(M)	50.457 MHZ 50.457 MHZ	40,454,575 MHZ 40,455,425 MHZ	40.000 MHZ 40.000 MHZ	454,575 KHZ 455,425 KHZ	457 KHZ 457 KHZ	2,425 HZ (SPACE) 1,575 HZ (MARK)
AFSK - 850 HZ SHIFT (LSB) 2,000 HZ CTR.	9.997,575 MHZ(S) 9.998,425 MHZ(M)	50.453 MHZ 50.453 MHZ	40,455,425 MHZ 40,454,575 MHZ	40.000 MHZ 40.000 MHZ	455,425 KHZ 454,575 KHZ	453 KHZ 453 KHZ	2,425 HZ (SPACE) 1,575 HZ (MARK)

C = CARRIER S = SPACE SB = SIDEBAND M = MARK

350-021A

Figure 5-1. Transceiver Reference and Synthesizer Frequencies (Sheet 2 of 2)

MIC audio mode since amplitude with a microphone can vary substantially from operator to operator, i.e., different operators peak at different voice levels.

d. Transmit Audio Clipper. Following the compressor circuit, the audio is routed to a clipper circuit. The clipper circuit is under operator control with the CLIP key, and can be enabled only in the USB, LSB and AME modes of operation. The clipper circuit is automatically bypassed in the CW and AFSK modes. Unlike the compressor circuit, the clipper circuit removes voice peaks to effectively raise the average RF output level. The clipper is adjustable internally from 0 to 12 dB.

e. Transmit Audio Balanced Modulator. The selected audio has one stage of buffering before application to a balanced modulator. Sidetone audio (a sample of the modulator input) is routed to the sidetone select circuit. The balanced modulator fully suppressed the 455 KHz carrier and has two sideband outputs, USB and LSB. The sidebands, due to the transceiver conversion scheme, are transposed. For example, if a 2 KHz tone modulates the 455 KHz carrier, the modulator outputs are 457 KHz (LSB) and 453 KHz (USB).

f. Transmit Audio 455 KHz IF. The nominal 455 KHz IF signal is routed to the IF filter assembly where the desired filter is selected based on the mode of operation. In the USB and AME modes the USB filter (451.950 - 454.650 KHz) is selected; in the LSB mode the LSB filter (455.350 - 458.050 KHz) is selected. The IF filters for AFSK operation are located on the AFSK assembly. Note the CW filter is centered at 455 KHz ± 200 Hz. For CW transmissions, a 1 KHz tone is injected at the balanced modulator. The balanced modulator carrier frequency is 454 KHz or 456 KHz, depending on whether CW-LSB or CW-USB is selected respectively. This results in an output from the balanced modulator of exactly 455 KHz, which is filtered as described above. Corresponding to the balanced modulator carrier offset, the synthesizer LO is also offset ±1 KHz so that actual transceiver transmissions are 1 KHz higher (CW-USB) or lower (CW-LSB) than the displayed transceiver frequency.

g. Transmit AME Audio. After filtering, the 455 KHz IF is applied to an Automatic Leveling Circuit (ALC) that attenuates the signal if the level is above the ALC threshold. When operating in the AME mode, the ALC circuit automatically reduces the USB input signal by 6 dB in the sideband control amplifier. Following the amplifier is the injection point for reinsertion of the 455 KHz carrier. In the AME mode, a carrier reduced by 6 dB is injected to combine with the reduced USB signal, creating the carrier +USB AM equivalent composite signal. The combining of two signals, each reduced by 6 dB, results in the same PEP as an individual signal at 0 dB.

h. Transmit 2nd TX Mixer. The nominal 455 KHz IF signal is amplified, sampled by the Transmitter Gain Control (TGC) circuit, and applied to the 2nd TX mixer. The TGC sample is used as a reference signal and is compared with a feedback signal from the RF output directional coupler. The error signal obtained by this comparison automatically corrects the RF power output level to keep the IF sample and the RF sample at a constant ratio. This comparison method allows the modulation envelope to be tracked, with the circuit responding only to actual gain changes. The output of the 2nd TX mixer is 40 MHz plus the nominal 455 KHz input. For example, if operating in the USB mode with a 2 KHz modulating tone, the IF input to the mixer is 453 KHz (455 KHz - 2 KHz) and the desired output of the 2nd mixer is 40.453 MHz. The 2nd TX mixer output is followed by a bandstop filter which eliminates undesired 39.545 MHz products of the up-conversion. The nominal 40 MHz IF signal is amplified and applied to a PIN diode attenuator which levels the signal through TGC action. The IF signal is then bandpass filtered by a crystal filter (40.450 - 40.460 MHz) and applied to the 1st converter mixer.

i. Transmit 1st TX Mixer. The output of the 1st converter mixer is the final transmit frequency in the range of 1.6 - 29.999,990 MHz. The synthesizer provides the local oscillator mixer input (42.055-70.45499 MHz). The mixer is followed by a 0-30 MHz low pass filter which removes unwanted mixer output products and spurious signals. The signal is then amplified and leveled by TGC action, resulting in an RF output of 100 watts into a 50 ohm load.

j. Transmit RF Output. The RF output is applied, via the T/R switch, to a low pass filter to remove frequency harmonics. The low pass filter assembly consists of six separate half-octave low pass filters that are selected automatically according to the transceiver frequency of operation. Following the filter, the RF output passes through a directional coupler that detects the forward and reverse power levels and is applied to an antenna. The antenna must represent a 50 ohm load impedance with a 2:1 VSWR or better, or the reverse power sample will

command the TGC circuit to reduce the output power to levels that will not damage the equipment. Equipment applications that do not use a 50 ohm antenna require an antenna coupler to convert the antenna impedance into the required 50 ohm load.

5-5. FUNCTIONAL OPERATION AND SIGNAL FLOW OF RECEIVING CIRCUITS. For the discussion of receiver circuits, refer to figure FO-1 in chapter 7.

a. Receiver Dual Conversion Function. A received signal between 1.6 and 29.99999 MHz is converted to a 40.455 MHz 1st IF frequency for rejection of interfering signals, and converted to a 455 KHz 2nd IF frequency for selectivity. The input signal is first routed through a half-octave low pass filter and 0-30 MHz low pass filter before application to the 1st converter mixer. A series limiter located just before the 0-30 MHz low pass filter limits any excessively strong signal, thereby protecting the receiver front end from damage. During the BIT self test sequence, a received signal is simulated at the RF input port, with the normal received signal disconnected for the duration of the BIT test.

b. Receive 1st IF Mixer. The local oscillator signal injected at the 1st converter mixer (42.055-70.45499 MHz) converts the input 1.6 - 29.999,990 MHz signal into an IF frequency at 40.455 MHz. The local oscillator signal is generated by the synthesizer. The nominal 40.455 MHz IF signal is bandpass filtered by a crystal filter (40.450-40.460 MHz) to remove image and spurious out-of-band signals. Following the crystal filter, the 40.455 MHz IF is amplified and leveled by an AGC PIN diode attenuator for application to the second mixer. Just before the second mixer is a bandstop filter that removes any second image signals.

c. Receive 2nd IF Mixer. The inputs to the 2nd mixer are a LO input of 40 MHz and the 40.455 MHz IF input. The output of the mixer is a nominal IF frequency of 455 KHz, which is filtered to remove any traces of undesired mixer output signals. The 455 KHz IF is then amplified and applied to the IF filter assembly. The IF filter selected depends on the operating mode. For the USB and AME modes, the 2.7 KHz LSB filter is selected; for the LSB mode, the 2.7 KHz USB filter is selected. Observe that the USB and LSB frequencies are transposed as required by the transceiver frequency conversion scheme. The CW filter is a 400 Hz bandpass filter and the AFSK mode uses filters located on the AFSK assembly. (The AFSK filter characteristics depend on the frequency shift selected.)

d. Receive Product Detector. The output of the IF filter is amplified and applied to an AGC amplifier. The gain of the AGC amplifier is dependent on the AGC envelope detector output that is amplified and shaped by the AGC circuit. Following the AGC amplifier is another stage of amplification followed by the product detector. The product detector can be thought of as a "mixer" for which the inputs are the nominal 455 KHz IF frequency and a reference 455 KHz frequency. The output of the "mixer" is the frequency difference between the inputs, i.e., the recovered audio modulation. An envelope detector is used in the AME mode. In the CW mode, a 454 KHz or 456 KHz carrier frequency is used at the product detector, as selected by the CW- LSB/CW-USB switch for CW. The output of the product detector, for a centered BFO, is a 1 KHz tone. The BFO feature can be used in any mode (except AME), when a frequency offset is desired at the product detector. For example, in CW operations, the detected 1 KHz tone can be raised or lowered by the operator if desired.

e. Receive Audio Squelch. The resultant audio from the product or envelope detector is sampled by the squelch circuit and metering circuit, and applied to the audio output terminals or front panel speaker. The squelch feature, which is adjustable and under operator control, is used to mute the audio output when there is no detected audio. Proper squelch adjustment eliminates constant background noise during periods of signal monitoring when nothing intelligible is being received.

f. Receive Audio. The audio levels are adjustable for the front panel speaker, the LINE output and PATCH receive outputs. The AUDIO 2 output is not adjustable. The squelch feature does not mute the LINE, PATCH or AUDIO 2 outputs. When the VOX feature of the transmitter is being used, an audio output sample prevents VOX action during signal reception. This is the antivox circuit feature, which has an adjustable threshold level controlled at the front panel.

5-6. FUNCTIONAL OPERATION AND SIGNAL FLOW OF SYNTHESIZER AND REFERENCE CIRCUITS. The synthesizer and reference injection frequencies, shown on figure FO-1 in chapter 7, are generated in the Synthesizer and Reference/BFO modules. Generation of the five

frequencies is illustrated in simplified form in figure 5-1. All reference and synthesized frequencies are based on a 10 MHz frequency standard input.

a. 100 Watt Transceiver Frequency Scheme. The 1st LO and carrier/BFO frequencies are under microprocessor control and are shifted to suit a particular mode of operation. In the USB or LSB mode, no shifts of either the 1st LO or the BFO are utilized; while in the CW mode, both the 1st LO and the BFO are shifted +/-1 KHz from their nominal position for CW-USB and CW-LSB, respectively. This permits use of a single centered IF filter for both modes. In AME, the 1st LO (and also the carrier in transmit) is shifted -400 Hz, thus allowing a carrier at the frequency entered on the transceiver front panel to pass through the USB filter for envelope demodulation. In the AFSK mode, the 1st LO and the BFO are shifted up or down depending on the selected AFSK shift. The 1st LO is offset by the shift center frequency; and the BFO is offset by 500 Hz, 1 KHz, or 2 KHz, also as a function of the selected AFSK shift. This technique facilitates demodulation of the various shifts and also permits centered filters to be used for both USB and LSB operational modes. Notice that in all modes the relative position of signals with respect to the center-tuned frequency is reversed in the 2nd IF from the relative position of the signals at the RF input.

b. 40 MHz Reference Generation. Generation of the 40 MHz signal is accomplished by passing the 10 MHz reference through a X4 multiplier, the output of which is a 40 MHz output.

c. 200 KHz Reference Generation. The 200 KHz reference is the input to the divide-by-N.F synthesizer circuit for generation of the 42.055-70.45499 MHz LO 1 signal. The 10 MHz is divided by 50 to create 200 KHz output.

d. 8 KHz Reference Generation. The 8 KHz reference output is generated by dividing the 10 MHz reference by 1250. A series of successive dividers are used. The 8 KHz reference is used by the Reference/BFO PWB for generation of the 455 KHz carrier and BFO frequencies.

e. 1 KHz Reference Generation. The 1 KHz reference is used as an audio tone for the BIT self-test sequence and for the modulation/sidetone audio feature used during CW operations. It is generated by dividing the 8 KHz reference output by 8 for the final 1 KHz output.

f. 455 KHz Reference/BFO Signals. The 455 KHz reference is used during receive as a BFO signal, and during transmit as a carrier signal. The BFO output is used at the product detector for demodulation of the USB and LSB modes. An envelope detector is used for AME. In the CW mode, the product detector reference is 454 KHz or 456 KHz, resulting in a detected tone of 1 KHz. It is possible to vary the reference with the Beat Frequency Oscillator (BFO) function. The reference can be varied ±1 KHz in 10 Hz steps. During transmit, the carrier signal is fixed at 455 KHz (no offset) for SSB modes, and 454 KHz or 456 KHz in CW (selectable), and used by the balanced modulator to generate the upper and lower sidebands. Also, it is used for carrier reinsertion in the AME mode (-6 dB level).

g. 455 KHz Reference/BFO Signal Generation. A phase lock loop technique is used in the generation of the 455 KHz signal. A nominal 45.5 MHz signal is first generated by the VCO and then divided by 100 to obtain the final output. The Voltage Controlled Oscillator (VCO) receives a dc voltage from the phase detector. The dc voltage is the exact amount required to generate a VCO frequency that divided by N will equal 1 KHz. Every output pulse from the divide-by-N circuit is compared in phase with the 1 KHz reference to derive a phase-error signal for controlling the VCO frequency, thus completing the loop. The VCO frequency is 45.5 MHz and the divide-by-N is 45,500 when there is no BFO offset. Offset is entered via the divide-by-N which is translated into the final frequency. For example, a divide-by-N of 45,600 will result in a 456 KHz output frequency.

h. 1st LO Generation. Generation of the 1st LO uses a single-loop fractional-N technique, generating an output frequency in the range of 42.055-70.45499 MHz. Frequency information from the microprocessor programs the divide-by-N.F circuit. Operation of the PLL is similar to operation of the Reference/BFO PLL circuit. The difference in the two loop techniques is the fractional divide-by-.F block. The divide-by-.F block, together with the swallow gate, allow the Synthesizer to generate frequencies that are non-integer multiples of the 100 KHz phase detector reference frequency. The Synthesizer is thus able to make frequency changes as small as 10 Hz. Injection of the 42.055-70.45499 MHz LO 1 converts a received signal in a 1.6 - 29.999,990 range to an IF of 40.455 MHz. In the transmit path, the 40.455 MHz IF is converted into the

final transmit frequency between 1.6 and 29.999,990 MHz.

5-7. FUNCTIONAL OPERATION AND SIGNAL FLOW OF TRANSCEIVER CONTROL CIRCUITS. Refer to figure 5-2 for the discussion of the transceiver control circuits. The Transceiver Control Board is the controlling element for the transceiver. It monitors the status of the front panel keyboard and directs the activity of the front panel displays. In addition, control and serial data are directed to and from various transceiver modules and their interfaces to place the transceiver in the desired mode of operation. The various activities of the control board are coordinated by a Central Processing Unit (CPU), which in turn follows the program instructions stored in memory.

a. Microprocessor Device. The Central Processor Unit is a type 8088 microprocessor. The 8088 has a 16-bit address bus interface, an 8-bit data bus interface, and a 16-bit internal architecture that incorporates the attributes of both 8 and 16-bit microprocessors. To reduce the 8088 to a 40- pin package, the address bits A0-A7 are time multiplexed with the data bus D0- D7. That is, terminals AD0-AD7 are sometimes used for addressing and sometimes for data. The CPU resolves the time multiplexing at the beginning of each program bus cycle by first using the AD0-AD7 pins for address, during which the CPU sends out an "Address Latch Enable" (ALE) strobe. The ALE strobe latches the address on lines AD0-AD7 into a device external to the CPU. After ALE, the eight terminals become a 2-way 8-bit data bus for the remainder of the program bus cycle.

b. Program Memory. The operating program (software) for the CPU is stored in three Eraseable Programmable Read Only Memory (EPROM) devices. The EPROM's are programmed by the factory and should not be changed by the user. Each EPROM has a memory format of 16Kx8, i.e., an input address of 14 bits identifies one of 16,384 locations in memory, the output of which is an 8-bit byte.

c. Data Memory. The CPU, in executing the program stored in the EPROM's, often needs to store data on a temporary basis. Temporary data storage is supplied by two Random Access Memory (RAM) devices with a memory format of 2Kx8. An input address of 11 bits identifies one of 2,048 locations in memory. Data is read from a RAM addressed location when the CPU issues a "read" command. Data can be written into the RAM addressed location when the CPU issues a "write" command. Battery backup is provided to allow for long term, non-volatile storage of radio status.

d. Memory and I/O Decoding. The CPU has output control signals "Data Transmit/Receive", "IO/Memory", "Read", "Write" and "Status Out". The control signals are combined with address bits to decode memory and Input/Output (I/O) devices. The three EPROM's and two RAM's are enabled individually by five memory decoding outputs as the CPU does not "see" individual memory devices, but rather, memory as a whole. The same holds true for the I/O devices, of which there are four: Module Control Bus (MCB), Interrupt Controller, Analog/Digital Converter, and Programmable Peripheral Interface. Through the I/O decoding, the desired I/O port is selected.

e. Microprocessor Reset. CPU program execution is halted and restarted if a "reset" command is generated. "Reset" is generated from any of four conditions;

(1) At power up.

(2) If +13.6 Vdc supply is low.

(3) If normal program execution is disrupted.

(4) If manual reset has been activated.

The reset signal is generated by a voltage comparator circuit. During normal operation of the transceiver, a reset signal is not generated.

f. Microprocessor Clock. The CPU input clock of 5 MHz is derived from a 15 MHz crystal oscillator output divided by three. The divider circuits have three other outputs: 2.5 MHz "Master Clock", 625 KHz "A/D Clock", and "Real Time Clock", which produces a pulse every 13.1072 milliseconds.

g. Microprocessor Ready. The CPU "Ready" input port is used to inject a "wait" state during a software bus cycle. A typical bus cycle requires four 5 MHz clock periods; T1, T2, T3 and T4. T3 and T4 are used for CPU data transfer. Relatively slow data devices (EPROM's and A/D converter) require additional time in the bus cycle to assure complete data transfer. The additional time is obtained by injecting a fifth pulse in the bus cycle, i.e., the complete cycle is T1, T2, T3, Tw (wait) and T4. The period Tw is established by the CPU "Ready" port from timing generated by ALE and

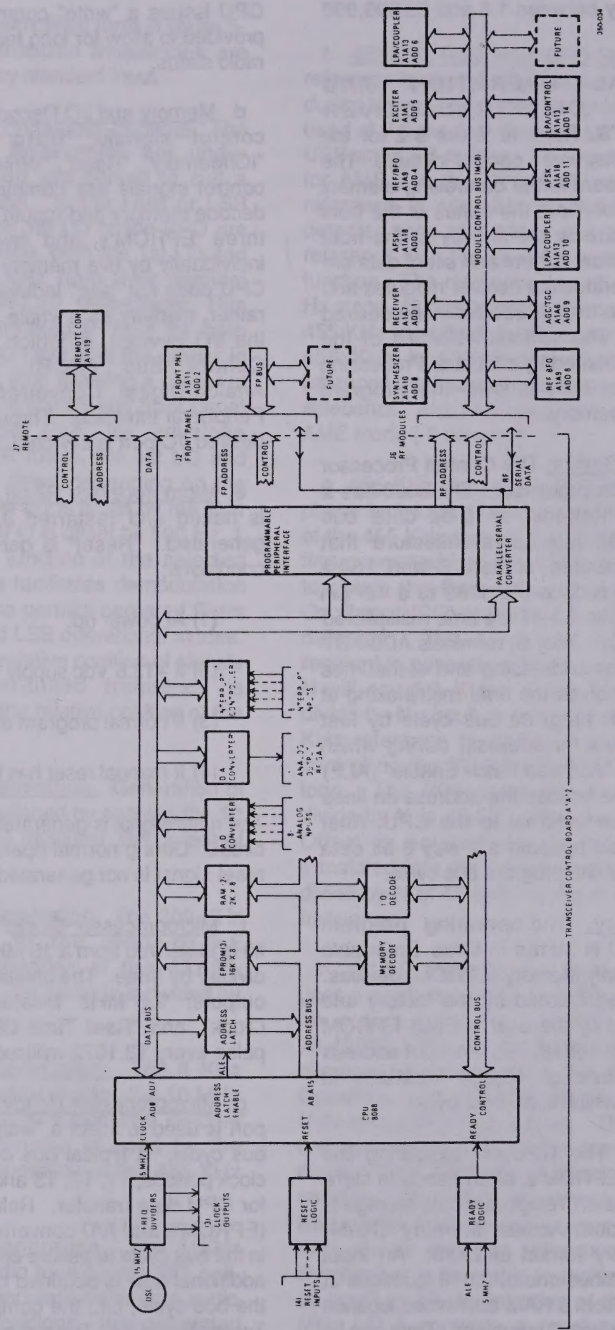


Figure 5-2. Simplified Transceiver Control Circuits

5 MHz clock pulses. Time Tw is injected in every bus cycle even though it is not always required.

h. Analog-to-Digital Conversion. The Analog-to-Digital (A/D) Converter has eight input signals. The A/D device has three address input bits to allow the CPU to select which of the inputs is to be converted. Six of the inputs are for the front panel meter display, one is a status signal for the CPU and the last is an operating parameter, RF GAIN. The operating parameter RF GAIN is converted to digital form only because of the required compatibility with the remote control unit where RF GAIN is interfaced digitally. When the transceiver is operated in the LOCAL mode, the RF GAIN analog parameter is converted to digital form and immediately reconverted back to analog. The eight analog inputs are:

(1) RF GAIN Operating Parameter

(2) Power Supply Status

(3) LOW PWR Meter

(4) V SIG Meter

(5) V FWD Meter

(6) V REFL Meter

(7) V AFSK Meter

(8) V AUDIO Meter

i. Digital-to-Analog Conversion. The Digital-to-Analog (D/A) element, as discussed above, is used solely for conversion of digital RF GAIN to analog RF GAIN. When operating in the REMOTE mode, the RF GAIN parameter is selected at the Remote Control front panel, converted to digital form at the remote interface, then routed to the transceiver in digital form. At the transceiver, the D/A device converts the digital signal from the remote unit back to RF GAIN analog. To maintain compatibility, the transceiver operating in LOCAL must also convert the signal to digital form and then immediately convert it back to analog form.

j. Interrupt Controller. CPU program execution is interrupted when the interrupt controller detects a condition that must be immediately serviced. The CPU reads in an 8-bit byte from the interrupt controller to identify the interrupt and determine what action is required. After servicing the interrupt, the CPU returns to the program position before the interrupt and continues processing. The interrupt controller has eight interrupt inputs:

(1) RF Module Attention - One of the modules on the Module Control Bus (MCB) requires CPU attention.

(2) Front Panel Attention - One of the front panel keys has been pressed and the CPU must service the request.

(3) Real Time Clock has occurred - Every 13.1072 milliseconds an interrupt is generated, which is used by software to keep track of real time.

(4) Key Down Condition - The CPU processes every keyline closure ('key' condition).

(5) Key Up Condition - The CPU processes every keyline opening ('unkey' condition).

(6) UART Ready to Receive - The CPU is advised when the system UART has completed reception of a serial frame from the remote control unit.

(7) UART Ready to Transmit - The CPU is advised when the system UART has completed transmission of a serial frame to the remote control unit.

(8) Remote Ready to Receive-Auxillary - (Not Used)

k. Programmable Peripheral Interface. The Programmable Peripheral Interface interfaces with a variety of control signals both to and from the CPU. One of the more important functions is to generate, under CPU control, an 8-bit word that is divided into 4-bit FP (front panel) and RF (radio frequency) portions. The FP and RF 4-bits can each address 15 modules. (The 16th state is a null condition.) Control functions, read, write, clock, etc., are routed to all modules, as is the I/O data. However, only the addressed module will respond to the CPU commands.

l. Parallel/Serial Converter. The "write" or "read" data for the FP or RF Module Control Bus is serial. Since the CPU data is 8-bit parallel, a converter is needed to convert parallel/serial data back and forth. For "write" operations, CPU data is loaded into the parallel/serial converter and then clocked out serially to the addressed FP or RF module. At the FP or RF

module, the serial data is loaded into an 8-bit register in parallel. In the opposite direction, 8 bits of parallel data are converted to a serial bit stream at the FP or RF module and are clocked into the control board parallel/serial converter serially. The loaded register is then read in as an 8-bit byte by the CPU. One of the main advantages of a serial data interface between the Control Board and the Front Panel and RF Modules is the elimination of individual parallel connectors for each module. In addition, option incorporation is simplified, since all that is required is connection to the bus and the use of an identifying module address. The FP and RF data lines are combined for the parallel/serial converter. Control signals and addressing prevent simultaneous operation of the two interfaces.

m. Module Control Bus. The data exchange between the CPU and RF modules takes place via the Module Control Bus (MCB). The MCB consists of a 4-bit address, read/write strobe, clock, attention line and serial data stream. The 4-bit address identifies which module on the MCB will communicate with the CPU. Some modules have more than one function, e.g, the Reference/BFO module. This accounts for more than one address being assigned to a single module. In addition, the routing of the MCB to modules is not always direct. For example, the Reference/BFO module is accessed via the Synthesizer module. The commands "Read" and "Write" determine the direction of the data flow with respect to the CPU, i.e., "Read" data flows into the CPU. "RF Attention" is a signal from an RF module that is used as an interrupt to inform the CPU that it has status to send to the CPU. The 625 KHz clock is derived from the 2.5 MHz master clock divided by 4.

(1) MCB "Write". In the "write" configuration, the MCB serial data stream is simultaneously clocked to all RF modules with a common "clock" signal. The "clock" pulses are counted out (modulo 8) in the exact number to transfer the required data. For example, if the data is intended for an RF module with four shift registers (each register holds an 8-bit byte), then exactly 32 clock pulses are produced. After the clock signal, the control board generates an MCB address, ADD0-ADD3, that is applied to all RF modules. The data is loaded into all module input registers, but only one RF module correctly decodes the address; i.e., the module for which the data is intended. Following the address, the control board puts out a "write" strobe which is also applied to all MCB RF modules but is only recognized by the selected module. Data that was loaded into all the RF module serial registers now latches into the storage register only for the selected module via the "write" strobe, and the data appears at the selected module shift register outputs in parallel.

(2) MCB "Read". In the "read" configuration, status signals are applied to shift register parallel inputs at all MCB RF modules. Typically, these are BIT inputs to advise the control board of the results of BIT testing. When the microprocessor software routine calls for an input from an MCB module, the control board generates an MCB address, AD0-AD3, that is applied to all RF modules. Only the selected module is able to decode the address. Following the address, the "read" strobe is generated, enabling only the selected module's parallel-to-serial device. The "read" strobe is generated concurrently with the "clock" signal, which clocks the parallel inputs at the module device serially into the control board register via the MCB. Only the exact number of clock pulses required to empty the module register are produced. For example, if an 8-bit parallel byte is to be transfered from a module to the control board, then only 8 clock pulses are generated.

n. Front Panel Bus. The Front Panel Bus operates in the same way as the RF Module Control Bus. It has a 4-bit address, although only a single module is addressed. The interrupt signal is "Front Panel Attention." This interrupt indicates that a key on the front panel keyboard has been depressed.

o. Remote Control Interface. When the Remote Control option is installed, selection of the "Remote Control" mode results in control of operating parameters from the Remote Control Unit rather than from the local front panel. The key device on the remote control board is the Universal Asynchronous Receiver/Transmitter (UART). Data is read to and from the UART, as determined by the Remote Control Interface Board's interrupts and control signals. Operator control resides with the remote control unit when the system is put in "remote."

5-8. FUNCTIONAL OPERATION AND SIGNAL FLOW OF POWER SUPPLY CIRCUITS. Refer to figure 5-3 for the description of the power supply circuits.

a Power Supply Voltages. The power supply circuits generate four output voltages required by the transceiver:

(1) +15 Vdc @ 1.8 amperes

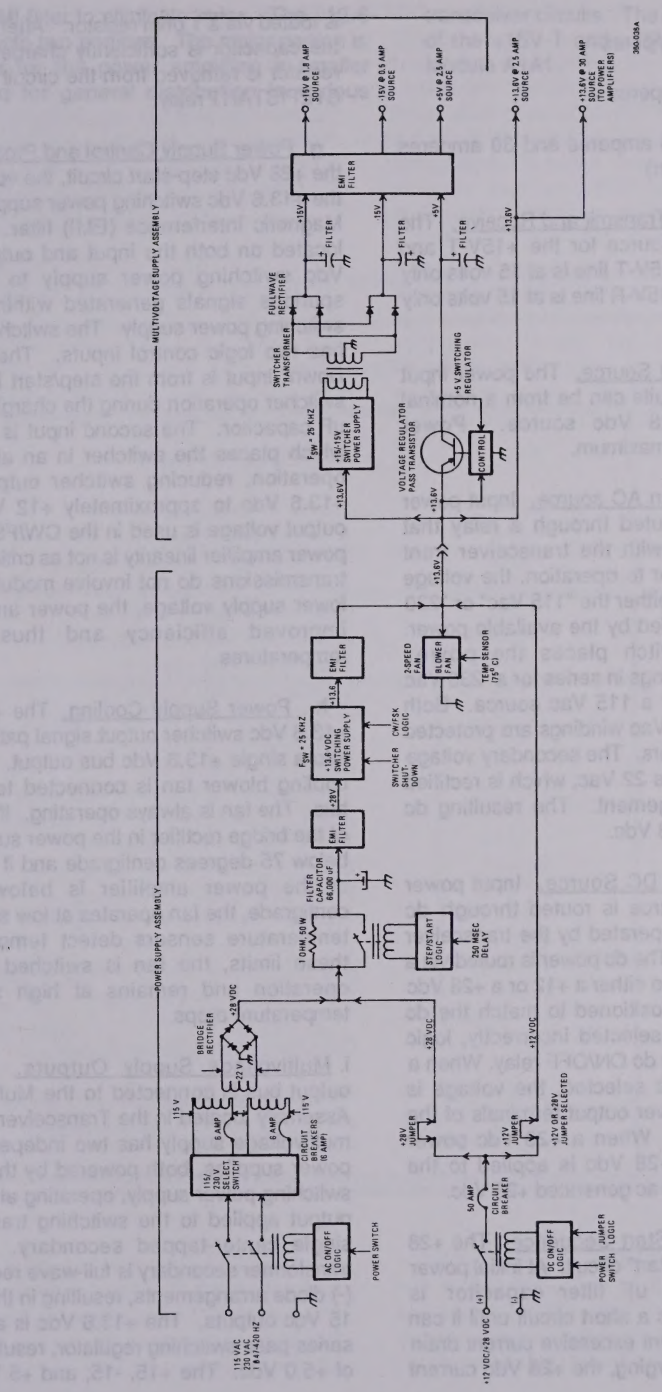


Figure 5-3. Simplified Transceiver Power Supply Circuits

(2) -15 Vdc @ 0.5 amperes

(3) +5 Vdc @ 2.5 amperes

(4) +13.6 Vdc @ 2.5 amperes and 30 amperes (for power amplifier)

b. +15 Supply During Transmit and Receive. The +15 Vdc supply is the source for the +15V-T and +15V-R supplies. The +15V-T line is at 15 volts only during transmit and the +15V-R line is at 15 volts only during receive.

c. Power Supply Input Source. The power input for the power supply circuits can be from a nominal 115/230 Vac or +12/28 Vdc source. Power consumption is 650 watts maximum.

d. Power Input From an AC source. Input power from an ac source is routed through a relay that operates in conjunction with the transceiver front panel power switch. Prior to operation, the voltage select switch is placed in either the "115 Vac" or "230 Vac" position, as demanded by the available power. The voltage select switch places the power transformer 115 Vac windings in series for a 230 Vac source and in parallel for a 115 Vac source. Both transformer primary 115 Vac windings are protected by 6 ampere circuit breakers. The secondary voltage of the power transformer is 22 Vac, which is rectified by a bridge diode arrangement. The resulting dc voltage is approximately 28 Vdc.

e. Power Input From a DC Source. Input power from a +12/+28 Vdc source is routed through dc ON/OFF relay, which is operated by the transceiver front panel power switch. The dc power is routed via a 50 ampere circuit breaker to either a +12 or a +28 Vdc jumper. The jumper is positioned to match the dc source. If the jumper is selected incorrectly, logic prevents the closure of the dc ON/OFF relay. When a +12 Vdc power source is selected, the voltage is applied directly to the power output terminals of the power supply assembly. When a +28 Vdc power source is selected, the +28 Vdc is applied to the same voltage buses as the ac generated +28 Vdc.

f. Power Supply Step-Start Sequence. The +28 Vdc is applied to a "step- start" circuit. At initial power application, the 60,000 uF filter capacitor is uncharged and represents a short circuit until it can begin to charge. To prevent excessive current drain during initial capacitor charging, the +28 Vdc current is routed via a 1 ohm resistor. After 250 milliseconds, the capacitor is sufficiently charged and the 1 ohm resistor is removed from the circuit by closure of the STEP/START relay.

g. Power Supply Control and Protection. Following the +28 Vdc step-start circuit, the voltage is routed to the +13.6 Vdc switching power supply via an Electro-Magnetic Interference (EMI) filter. An EMI filter is located on both the input and output of the +13.6 Vdc switching power supply to attentuate any spurious signals generated within the +13.6 Vdc switching power supply. The switching power supply has two logic control inputs. The "Switcher Shut Down" input is from the step/start logic; it prevents switcher operation during the charging of the 60,000 uF capacitor. The second input is "CW/FSK" logic, which places the switcher in an alternate mode of operation, reducing switcher output voltage from +13.6 Vdc to approximately +12 Vdc. The lower output voltage is used in the CW/FSK modes where power amplifier linearity is not as critical (CW and FSK transmissions do not involve modulation). With the lower supply voltage, the power amplifier runs with improved efficiency and thus with cooler temperatures.

h. Power Supply Cooling. The +12 Vdc input or +13.6 Vdc switcher output signal paths are combined into a single +13.6 Vdc bus output. A power supply cooling blower fan is connected to the +13.6 Vdc bus. The fan is always operating. If the temperature of the bridge rectifier in the power supply assembly is below 75 degrees centigrade and if the temperature of the power amplifier is below 85 degrees centigrade, the fan operates at low speed. When the temperature sensors detect temperatures above these limits, the fan is switched to high-speed operation and remains at high speed until the temperature drops.

i. Multivoltage Supply Outputs. The +13.6 Vdc output bus is connected to the Multivoltage Supply Assembly located in the Transceiver Assembly. The multivoltage supply has two independent switching power supplies, both powered by the +13.6 Vdc. A switching power supply, operating at 25 KHz, has an output applied to the switching transformer with a single center-tapped secondary. The switching transformer secondary is full-wave rectified by (+) and (-) diode arrangements, resulting in the +15 Vdc and -15 Vdc outputs. The +13.6 Vdc is also applied to a series-pass switching regulator, resulting in an output of +5.0 Vdc. The +15, -15, and +5 Vdc outputs are

routed to an EMI filter to eliminate noise. The +13.6 Vdc is divided into two portions. The major portion is primary power for the power amplifier; a smaller portion is used for general distribution in various transceiver circuits. The devices used for generation of the +15V-T and +15V-R sources are on Exciter Module A1A1.

Section II. FUNCTIONAL OPERATION OF ELECTRONIC CIRCUITS

5-9. INTRODUCTION. Individual paragraphs are dedicated to each transceiver module or assembly. This approach is compatible with the BIT approach to trouble isolation and replacement by assemblies. Text is supported by block diagrams, logic diagrams, timing diagrams and simplified schematic diagrams. These paragraphs assume the operator/technician is familiar with the information given in section I of this chapter. Each module, assembly and sub-assembly in the transceiver is assigned a reference designator forming a "family tree" of assemblies. The illustration for the "family tree" is given in drawing FO-2 found in chapter 7. A summary of the reference designators is given in table 5-1.

Table 5-1. Transceiver Assembly Reference Designators

Paragraph	Designation/Assembly	
5-11	A1	Transceiver Assembly
5-15	A1A1	Exciter PWB Assembly
5-18	A1A2	IF Filter PWB Assembly
5-21	A1A3	1st Converter PWB Assembly
5-24	A1A4	100 Watt PA Assembly
5-27	A1A5	Low Pass Filter PWB Assembly
5-33	A1A6	AGC/TGC PWB Assembly
5-40	A1A7	Receiver PWB Assembly
5-44	A1A8	Crystal Oscillator Assembly
5-48	A1A9	Reference/BFO PWB Assembly
5-53	A1A10	Synthesizer PWB Assembly
5-57	A1A11	Front Panel Assembly
5-60	A1A12	Transceiver Control PWB Assembly
5-70	A1A13	LPA/Coupler Interface PWB Assembly
5-73	A1A14	Multivoltage Supply Assembly
5-76	A1A15	Interconnect PWB Assembly
5-78	A1A16	Audio Interface PWB Assembly
5-81	A1A17	Coupler Connector PWB Assembly
5-83	A1A18	AFSK Module Assembly
5-89	A1A19	Remote Control Interface PWB Assembly
5-90	A1A20	Connector Plate Assembly
5-91	A2	Cover Assembly (Power Supply)
5-94	A2A1	Power Supply Protection and Control Assembly
5-97	A2A2	+13.6 Vdc Power Supply Assembly
5-100	A2A3	EMI Filter Assembly

5-10. OVERALL ASSEMBLY DESCRIPTIONS. The paragraphs in section II follow the sequence in table 5-1. 100 Watt Transceiver Assembly and Power Supply Assembly discussions include overall assembly interconnection information. The physical locations of individual assemblies in the transceiver are illustrated in figure 1-3. All parts list and component information for the Transceiver and Power Supply units is provided in the Depot Manual listed in Table 1-6.

5-11. TRANSCEIVER ASSEMBLY A1, 10085-0100. The Transceiver Assembly, A1, houses all "A1" designated transceiver modules as listed in table 5-1. With the exception of the front and rear panel connectors, all A1 connectors are mounted directly on the assemblies. The assemblies are then interconnected through a series of ribbon and coaxial cables. A complete interconnection schematic is supplied in the associated Depot Manual.

5-12. INTERCONNECTION CABLES. Interconnection cables fall into two catagories: cables that are permanently attached at one end to the associated assembly (pendant cables) and cables that interconnect at all (two or more) ends (cable assemblies). Cable assemblies are given a "W" designation, i.e., A1W1, A1W2, A1W3, etc., and are listed in table 5-2.

5-13. SIGNAL TRACING IN TRANSCEIVER. Signal tracing in the Transceiver Assembly is accomplished by cross referencing between Transceiver Assembly, A1, Schematic Diagram, and various Module/Assembly Schematic Diagrams. All schematic diagrams used for signal tracing are located in the Depot Manual.

5-14. DESCRIPTION OF CABLE ASSEMBLIES. The "W" designated cables are described below in tabular form. Each cable assembly is identified with a "W" number, e.g., W2, W13, etc., and assigned an end condition designator, e.g., W2P1, W11P5, etc. This information is supplied to allow immediate connection information for separate cable assemblies. The pin call-out information for multi-pin cables is supplied in the Depot Manual.

Table 5-2. Transceiver Assembly Interconnection Cable Descriptions

Cable	Designator	Destination	Note
W1	W1P1 W1P2	A1A7J2 A1A2J1	COAXIAL CABLE
W2	W2P1 W2P2	A1A7J5 A1A2J2	COAXIAL CABLE
W3	W3P1 W3P2	A1A7J1 A1A3J2	COAXIAL CABLE
W4	W4P1 W4P2	A1A3J1 A1A5J3	COAXIAL CABLE
W5	W5P1 W5P2	A1A3J4 A1A4J6	COAXIAL CABLE
W6	W6P1 W6P2	A1A3J3 A1A1J3	COAXIAL CABLE

Table 5-2. Transceiver Assembly Interconnection Cable Descriptions (Continued)

Cable	Designator	Destination	Note
W7	W7P1	A1A5J2	COAXIAL CABLE - REAR PANEL
	W7P2	A1J1	CONNECTOR "RF INPUT/OUTPUT"
W8	W8P1	A1A5J4	COAXIAL CABLE - REAR PANEL
	W8P2	A1J2	CONNECTOR "RF SAMPLE"
W9	W9P1	A1A5J1	COAXIAL CABLE
	W9P2	A1A4J7	
W10	W10P1	A1A1J7	RIBBON CABLE - 34 PINS
	W10P2	A1A11A1J4	RIBBON CABLE - 20 PINS
	W10P3	A1A12J3	RIBBON CABLE - 14 PINS
W11	W11P1	A1A12J6	RIBBON CABLE - 10 PINS
	W11P2	A1A7J8	RIBBON CABLE - 10 PINS
	W11P3	A1A1J8	RIBBON CABLE - 10 PINS
	W11P4	A1A10J3	RIBBON CABLE - 10 PINS
	W11P5	A1A15J3	RIBBON CABLE - 10 PINS
	W11P6	A1A13J1	RIBBON CABLE - 10 PINS
W12	W12P1	A1A1J10	RIBBON CABLE - 50 PINS
	W12P2	A1A15J7	RIBBON CABLE - 30 PINS
	W12P3	A1A16J1	RIBBON CABLE - 10 PINS
	W12P4	A1J4	J4 REAR PANEL "AUDIO 2" - 9 PINS
W13	W13P1	A1A9J2	COAXIAL CABLE
	W13P2	A1A8J1	(P/O 9-PINS AT J10)

5-15 EXCITER PWB ASSEMBLY A1A1, 10085-5400. This manual portion describes Exciter PWB A1A1 as an individual assembly. Section I of this chapter describes the function of the Exciter PWB in relation to overall 100 Watt Transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagrams — Figures FO-3 to FO-6

b. Schematic Diagram — Depot Manual

c. Parts List — Depot Manual

d. Component Layout — Depot Manual

e. 100 Watt Transceiver Simplified Block Diagram — Figure FO-1

f. Overall Interconnection — Figures FO-11, FO-12

g. Transceiver Assembly Schematic Diagrams — Depot Manual

5-16 OVERALL EXCITER PWB FUNCTION. The Exciter Board has four primary functions, each of which is discussed below. A simplified diagram is provided for each discussion. For a detailed technical description of the Exciter Board, refer to paragraphs starting at 5-17.

a. Audio Select and Convert to 40 MHz IF Discussion. Refer to Figure FO-3 for the audio select/40 MHz IF discussion. All transmit audio sources are routed to the Exciter Board for selection and processing. On the Exciter Board, the audio inputs are microprocessor selected as inputs to a summing amplifier. A typical path is the microphone audio path.

(1) Microphone audio from the 100 Watt Transceiver front panel HANDSET/MIC connector is routed, via an amplifier, to a switch controlled by uP1, "MIC Audio Select". When the operator selects MIC audio, the switch is closed. The audio is levelled by a Voltage Controlled Amplifier (VCA) with a control input from the 100 Watt Transceiver front panel MIC adjustment.

(2) The MIC audio is sampled after the VCA for the Selected TX Audio meter input, and routed to an amplifier. After amplification, the MIC audio is automatically routed to an audio compressor circuit.

(3) The MIC audio can be routed through a clipper circuit that removes voice peaks. This is selectable at the 100 Watt Transceiver front panel as the CLIP feature. The threshold of the CLIP feature is adjustable. After amplification, the audio is applied to a balanced modulator.

(4) During CW operations, the 1 KHz audio is routed to the front panel speaker for a sidetone function (when the CW key is closed, the operator hears the sidetone). During BIT testing, a 1 KHz tone is injected into the MIC audio path for BIT detection.

(5) Prior to application of the MIC audio to a balanced modulator, a null adjust network is used to remove any carrier that may appear at the output of the balanced modulator. The carrier input to the balanced modulator is a 455 KHz reference for the MIC audio selection. (In CW, the carrier input is 454 or 456 KHz depending on the desired sideband output.) The 455 KHz carrier is switched with a "Carrier Enable" signal generated from the PROM keyline decoder (as discussed in the keyline section).

(6) The output of the balanced modulator is filtered on IF Filter Assembly A1A2 and returned to the Exciter Board for processing. The balanced modulator output is detected by a BIT control circuit (the injected 1 KHz signal is detected) and a logic signal, uP101, "455 KHz Modulation Detector BIT" is the output.

(7) The filtered 455 KHz is applied to an ALC PIN diode and a variable gain amplifier. The ALC circuit is used to remove fast rising 455 KHz peaks. The variable gain amplifier has two gain characteristics: 0 dB and -6 dB. The reference gain level is reduced to -6 dB when the AME operating mode is selected. This is required in order to combine the AME sideband signal (USB) with carrier (also reduced 6 dB), resulting in a combined signal that is 0 dB PEP. For the 455 KHz IF MIC audio, the amplifier operates at the 0 dB reference level.

(8) The 455 KHz IF is applied to a summing point where 455 KHz carrier, if any, is injected. Control signal uP21, "CW/SSB", is used to enable the 455 KHz carrier path. The carrier level is determined by a fixed voltage divider for -6 dB which is the level required for AME injection.

(9) The carrier level is further reduced by voltage divider resistors in the circuit. The other injection levels are adjustable. For example, selection of "Coupler Tune Select" (uP19) reduces the carrier level to approximately -6 dB. This level of carrier reduces the 100 Watt Transceiver output to 25 watts, which is the level required to tune an associated antenna coupler. (The AN/URA-38 ( ) antenna coupler requires an LPA to derive its required tune power.)

(10) The SSB or CW signal is amplified and applied to the 2nd TX Mixer for up conversion to a 40.455 MHz IF.

(11) The 455 KHz is envelope detected prior to application to the 2nd TX Mixer and exits the Exciter Board for application to the AGC/TGC Board. The envelope is also routed to two voltage comparators. The voltage comparator level switches when the 455 KHz envelope exceeds a threshold level. This charges capacitor C93 to a voltage that is amplified and applied to the ALC PIN diode, which turns on causing the excessively high envelope signal to be reduced.

(12) The ALC capacitor discharges through a fixed resistor and a switched resistor. The switched resistor reduces the time constant for C93 as determined by voltage comparator AR-13. The change in time constant configures the ALC loop for a variety of operating modes.

(13) The 40 MHz Local Oscillator (LO) is routed into the 2nd TX Mixer via an amplifier that is powered by +15V-T; that is, the amplifier is powered by +15 V only during periods of transmission. The output of the 2nd TX Mixer contains both the sum and the difference frequencies of the input signals. A crystal filter removes the unwanted "difference" output (nominal 39.545 MHz) and the desired "sum" output (nominal 40.455 MHz) is routed to the Transmitter Gain Control (TGC) PIN diodes.

(14) The input TGC control turns on the TGC diodes and the 40.455 MHz IF signal is attenuated. The attenuation level correlates to the desired 100 Watt Transceiver RF output level and power corrections are made automatically with TGC. Following TGC levelling, the signal is amplified using an amplifier controlled by +15V-T. The signal is thus blocked unless the 100 Watt Transceiver is in the transmit mode. The 40.455 MHz IF is then sampled by the uP100, "40 MHz Modulation Detector BIT" circuit, and the 40.455 MHz IF exits the Exciter Board.

b. Keyline Select Discussion. Refer to figure FO-4 for the discussion of Keyline Select. All system keylines enter the Exciter Board for processing. The CW keyline inputs are from a CW key connected to the front panel jack. When operating in LOCAL, the local CW key is connected; when operating in remote, the uP CW Key is connected. Both CW keylines are buffered. The local CW key is selected by control signal uP0, "CW Audio Select", and combined with uP CW Key. The uP CW is selected by microprocessor handling prior to application to the Exciter Board. The CW keyline is sampled by "CW Key", which is used for switching the 1 KHz audio signal for the sidetone and audio derived CW carrier signal.

(1) The VOX keyline is generated by sampling the MIC, AUDIO 2 and PATCH audio sources. When the 100 Watt Transceiver operator selects the VOX feature, the selected audio source is amplified by a Voltage Controlled Amplifier (VCA), the threshold level for which is determined by 100 Watt Transceiver front panel control, VOX. The audio is then converted into a +dc signal level.

(2) Front panel speaker audio is sampled and routed to the antivox VCA. The threshold level of this VCA is controlled by front panel control, ANTIVOX. The antivox output is converted into a -dc signal level. The VOX and ANTIVOX dc levels are combined and compared in a VOX voltage comparator. If the overall signal is below the VOX comparator reference level, then front panel speaker audio is present and the antivox feature prevents transmitter keying during periods of receiving. When the overall dc level is above the threshold level, then VOX keying is enabled via the VOX comparator. Adjustments of the VOX and ANTIVOX front panel controls allow the operator to adjust circuit action to suit any particular equipment application.

(3) The CW and VOX keylines are combined and applied to the keyline comparator. The keyline comparator does not switch until the capacitor at the inverting input discharges below a threshold level. The time constant forms the "hang time" for keyline action, i.e., the transmitter does not fully unkey until the hang time expires. The hang time is adjustable through resistor selection. Control uP9, "VOX Data Delay", places a low value resistor in parallel with C and the time constant is fixed and short. Control uP8, "VOX Voice Delay", places an adjustable resistor in parallel with C that permits varying the hang time over a wide range. Control uP0, "CW Audio/Keyline Select", also inserts an adjustable resistor that permits a wide variation in the hang time. Control signal, uP12, "TX Inhibit", places a small fixed resistor in the circuit to assure that when the 100 Watt Transceiver is disabled, the VOX keyline will not be enabled by a stray charge.

(4) The processed VOX/CW keyline is buffered and switched by control signal uP11, "VOX Keyline Select". Other keyline inputs are similarly switched except for EXT (external) Key, which can override any other selected keyline. The combined keyline is then "debounced" using an RC combination at the input to the PROM keyline Decoder. The debouncing circuit adds a small amount of delay in keyline action. The delay can be removed by shorting out the C element via a switch using control signal uP5, "AFSK Audio Select". For most equipment applications, this is not required, and the selection jumper is grounded.

(5) Other inputs to the PROM keyline decoder include "TX RF Mute", "uP Self Key" (Self Key is the operator selected keyline at the 100 Watt Transceiver front panel, TX KEY), "TX Inhibit" and a feedback keyline from the +15V-T/R control. The PROM generates outputs, "Carrier Enable", "Conditioned Key", "Raw Key", and "+15V-T/R Control". The keyline outputs are used on the Exciter Board and routed to other 100 Watt Transceiver modules. The +15V-T/R output is used to switch the +15 V supply during transmit for +15V-T (+15V only during transmit) and +15V-R (+15V only during receive).

c. Audio and RF Power Meter Selection. Refer to FO-5 for the discussion of Audio and RF Power Meter Selection. RF output level samples from the 100 Watt Transceiver (or the associated LPA) are switched using control signal uP16, "XCVR/LPA VSWR Meter Select". The selected level is routed to the front panel meter. The meter positions are FWD (forward),

REF (reflected), and VSWR (voltage standing wave ratio).

(1) The Vfwd output also provides an input to the Low Power Indicator circuit where a voltage comparator, with adjustable threshold, illuminates the front panel indicator for low power levels. The conditioned key control signal assures that the indicator will not illuminate during 100 Watt Transceiver receive periods.

(2) A set of switches and control signals select the front panel meter scales AUDIO, LINE, and PATCH. The meter scales indicate either the transmit level or receive level, as selected by control signal, "Conditioned Key". The AUX RX Audio signal is levelled by a VCA using front panel control, PATCH RCV. The signal is sampled for the metering circuit and exits the board. The selected meter audio is rectified and filtered to obtain a dc level. The dc level is converted from analog to digital form on the Control Board and processed to illuminate the desired meter segments.

d. Module Control Bus (MCB) Interface Discussion. Refer to figure FO-6 for the MCB discussion. The control signals for the Exciter Board are read into the assembly as a serial data stream, consisting of 32 bits of information. The MCB address strobe is coded for the Exciter Board and AGC/TGC Board by addresses 0101 (5) and 1001 (9), respectively.

(1) When MCB data is intended for the Exciter Board, decoding generates the desired enables for the bus registers. The clock signal then clocks 32 serial bits of data into the 32 bus register ports. After entry, the first data bit resides in the last bus register port and is used as part of the Exciter MCB BIT test sequence. After all data is clocked in, the "write" strobe is decoded. The data in the bus registers is latched into the bus storage registers and appears at the bus register output pins as steady control voltages.

(2) Twenty-one of the control outputs in the bus registers are assigned "uP" designations (e.g., uP3) and are routed to various locations on the Exciter Board. Using these control signals, the microprocessor selects the various signal paths, enables, keylines, and audio lines required to provide the desired modes of operation. Additional bus register outputs are routed to the power supply and low pass filter to control their functions.

(3) Data from the Exciter Board is sent to the control board via an 8-bit parallel-to-serial converter. While the microprocessor is performing the read function, the eight inputs to the parallel/serial register are read serially into the Control Board. The proper enables and "read" strobes originate from the decoder chip. The 8-bit word consists of BIT results, not only from the Exciter Module, but from the Power Amplifier (PA), AGC/TGC, and Low Pass Filter (LPF) as well.

5-17 DETAILED EXCITER BOARD CIRCUIT DESCRIPTIONS. The paragraphs below provide detailed descriptions of the Exciter Board circuits. Each description heading includes a reference designator, e.g., U12, Q17, etc., that identifies the circuit under discussion. The information flow corresponds to the Exciter Board schematic diagram starting with sheet 1 and continuing to the last sheet. The detailed information assumes the overall Exciter Board function is understood from the simplified descriptions provided in earlier paragraphs.

a. 1 KHz Audio Select U11A.

(1) The 1 KHz audio reference, entering the exciter board at J4, is used as the audio source for BIT testing, as the reference tone for audio-derived CW, and as the sidetone audio during CW transmissions.

(2) Switch U11A is operated by control signal uP7, "1 KHZ AUDIO SELECT". The switch is closed only during BIT testing. During the BIT sequence (which uses the MIC audio circuit path), the injected 1 KHz is used to modulate the 455 KHz carrier, which is then converted to the 40.455 MHz IF frequency.

b. 1 KHz Switching U2B, and U3A.

(1) The 1 KHz audio reference signal, used for audio-derived CW and sidetone, is switched by U2B,C as commanded by the "Combined CW Keyline". The "Combined CW Keyline" is the combined local and remote CW keyline. When the CW key is closed, the U2B,C switches close and the 1 KHz audio passes to switch U3A.

(2) The control signal for switch U3A is uP0, "CW Audio/Keyline Select". This switch is closed only when the 100 Watt Transceiver is operating in the CW Mode. The output of the switch is applied to the input of Operational Amplifier AR3A-2, which is the summing point for all 100 Watt Transceiver selected audio.

c. MIC Audio Select U5A.

(1) The front panel HANDSET/MIC input is routed to the Exciter Board via J9. The input audio is amplified by low noise FET amplifier AR1. Included in this audio path is the 1 KHz used in BIT testing. When the operator has selected audio source AUDIO: MIC, switch U3B is closed (also closed automatically in BIT) and audio is routed to voltage controlled amplifier U5A.

(2) The gain of amplifier U5A is dependent on the level of the 100 Watt Transceiver front panel "MIC" gain adjust potentiometer. The output of U5A is applied to the audio summing point at AR3A-2.

d. AUDIO 2 Audio Select U4B. The AUDIO 2 audio is a 600-ohm balanced input. The input is applied to a pad, formed by R297-R300, and coupled by T1. The AUDIO 2 audio is levelled by variable resistor R29 and applied to voltage follower AR2B-3. The voltage follower configuration provides isolation and impedance matching, but no gain or loss. When the operator has selected the audio source, AUDIO: AUDIO 2, switch U4B closes as commanded by control signal uP3, "AUDIO 2 Audio Select". The resulting audio is applied to audio summing point AR3A-2.

e. Patch Audio Select U7A. The Patch (Tx phone patch) audio is applied to voltage controlled amplifier U7A. The gain of U7A is determined by the input control voltage PATCH XMIT from the 100 Watt Transceiver front panel. The patch audio is then routed to select switch U4C-13, which is controlled by the operator when AUDIO: PATCH is selected at the 100 Watt Transceiver front panel. The U4C control voltage is uP4, "Patch Audio Select". The output of U4C-14 is applied to audio summing point AR3A-2.

f. AUX TX (AFSK) Audio Select U3C. Auxiliary AUX audio (typically, AFSK tones) is selected by U3C. The control voltage is uP5, "AFSK Audio/Keyline Select". The output of U3C-4 is applied to audio summing point AR3A-2.

g. Line (Remote) Audio Select U4A. Line Audio (typically remote audio) is selected by U4A. The control voltage is uP2, "Remote Audio Select". The output of U4A-4 is applied to audio summing point AR3A-2.

h. Audio Amplifier AR3A. The input to AR3A-2 is the summation point for the selected audio signal.

i. VOX Audio Amplifier AR4A. The VOX circuit generates a keyline when an audio level is detected. The input audio to the VOX circuit is from one of three sources: MIC, AUD2 and PATCH. The switched outputs from these audio sources are routed via resistors R52-R54 to the input of AR4A-6. The output of AR4A is routed to the VOX circuitry.

j. AUX Level Adjust U7B. Auxiliary audio enters the Exciter Board from two locations and is combined at capacitor C11. Typically, the auxiliary input is the received telephone patch audio. Auxiliary audio is then applied to Voltage Controlled Amplifier U7B-3 with a control input from the 100 Watt Transceiver front panel potentiometer, PATCH RCV. The output of U7B-7 is amplified by Operational Amplifier AR6A and exits the exciter board via R32 and C10.

k. Meter Select Switching U18A, B, C and U17C.

(1) The 100 Watt Transceiver front panel audio meter displays AUDIO, LINE, and PATCH levels. The switching signals originate from the front panel METER select function and conditioned key line. The LINE and PATCH signals have both transmit and receive inputs. Switch U18B selects either Line TX or Line RX audio; switch U18A selects either Patch TX or Patch RX audio. The control signal for U18A, B is the "Conditioned Keyline." Switch U18C is used to select either the PATCH or LINE audio and is operated by control signal uP17, "Line/Patch Meter Select".

(2) The selected PATCH or LINE audio is routed to switch U17C. U17C switches between PATCH/LINE and AUDIO meter positions. The control signal for U17C is uP15, "Line/Audio Meter Select". The audio input for the U17C-3 AUDIO is via Operational Amplifier AR3B. AR3B-5 samples the "Selected TX Audio" line via C36 and levels the signal with variable resistor R47.

l. Meter Audio Amplifier AR11B. The audio selected by devices U18A,B,C and U17C is amplified by Operational Amplifier AR11B and rectified by diode CR40. Capacitor C127 filters the dc voltage, which is limited to +4.7 V by zener diode VR3. The voltage that exits the exciter board at J7-21 is therefore a dc representation of the selected audio signal level. The dc voltage is converted into a digital 8-bit word by an analog-to-digital converter on the

A1A12 control board and applied to the digital front panel meter segments.

m. Audio Compressor U10. The selected TX audio is routed via switches U9A,B to an audio compressor circuit. The compressor circuit is bypassed except for audio select mode uP1 ("MIC Audio Select"). The U10 compressor device compresses 40 dB of audio range (variations) into ±1 dB range. The circuit exhibits a fast attack (2 milliseconds via C39)/slow decay (4 seconds via C38) characteristic. The slow decay characteristic prevents an increase in noise level during pauses in the microphone speech pattern. Operational Amplifier, AR7A, with the feedback network R84/R85/C44, bandlimits the audio signal. RF suppression is provided by C43. The compressed audio is applied to U9B-1 and routed to the audio clipper.

n. Audio Clipper AR8A,B.

(1) The clipper circuit is controlled by the operator via the 100 Watt Transceiver front panel CLIP control. When the CLIP feature is selected via control signal uP6, "Clip Select", the audio is routed first to Operational Amplifier AR8A. The audio input is amplified by AR8A and then adjusted with variable resistor R91. The clipper level can be adjusted from 0 dB (no clipping, R91 at minimum resistance) to 12 dB (maximum clipping, R91 at maximum resistance).

(2) Clipping action takes place in diode package CR10. The clipping threshold is 1V peak-to-peak at the diode common terminal as determined by R93 and R94. The clipped audio is applied to active filter AR8B which limits the harmonics generated during clipping and shapes the audio waveform for application to switch U11A-3 and then to voltage follower AR9A.

(3) Voltage follower AR9A provides a low impedance output for the final processed audio.

o. Balanced Modulator U12.

(1) Processed TX audio is applied to balanced modulator U12 to generate the upper and lower sideband signals. Input audio is routed through a precision resistor network that sets the modulator bias. Input carrier is routed via PIN diode switch CR11. The carrier signal is blocked unless CR11 is turned on. The control signal for CR11 is "Carrier Enable", the generation of which is discussed for device U15. When "Carrier Enable" is +15 V, CR11 is turned on (the ground return path is through R119) and carrier is applied to the modulator via a precision resistive network. The resistive network is used to bias the modulator. Variable resistors R110 and R117 are used to null out any carrier component at the modulator output. The two adjustments, R110 and R117, are interactive.

(2) The output of the modulator is balanced, with a center-tapped signal ground provided by resistors R103/R104 and capacitors C53/C54. One portion of the 455 KHz IF output exits the Exciter Board through an impedance matching network via connector P1. The other portion of the 455 KHz IF output is amplified by Q2 and rectified by CR13 and CR14. When modulation is present, the dc output of the rectifiers turns on transistor Q3 and the output of uP101 is at ground potential, i.e., "455 KHz Modulation Detector" BIT output is logic 0. During BIT testing, a 1 KHz tone is injected to generate the detected modulator sideband outputs.

p. 455 KHz Input Amplifier Q4/Q5. After filtering, the 455 Hz IF enters the Exciter Board at P2 and is applied to a pi pad for impedance matching and isolation. The signal is levelled through ALC action on PIN diode CR15. Amplifier Q4 has two gain characteristics: 0 dB for all modes except AME, and -6 dB when operating in the AME mode. AME requires the 455 KHz IF USB signal to be reduced to half voltage so that, in combination with a -6 dB reinserted carrier, the resultant signal is 0 dB PEP. Switching between gain modes is accomplished by control signal uP20, "AME Select". When not in AME, uP20 (logic high) switches precision resistor R144 in parallel with R134, thus setting the Q4 0 dB gain reference level. When AME is selected (logic low) PIN diode CR18 is turned off, resistor R144 is no longer in the circuit, and the gain of the stage is reduced by 6 dB. Transistor Q5 further amplifies the signal and applies the 455 KHz IF to the base of Q6.

q. 455 KHz Carrier Reinsertion Q8.

(1) The reinsertion of 455 KHz carrier is accomplished via transistor Q8, which is turned on by a control signal uP21, "CW/SSB Select". The control signal also enables PIN diode switch CR12. With uP21 activated, carrier is reinserted at Q6 at one of three levels, depending on the selected mode: AME mode (-6 dB), Tune Power (-4.5 dB), and Pilot Carrier suppressed (PCS) (-20 dB). All carrier levels are referenced to a full CW carrier.

(2) For the AME mode, there is no control signal and the carrier level of -6 dB is determined by R150. The -6 dB carrier is then combined with the -6 dB 455 KHz IF, yielding a combined signal that is 0 dB PEP.

(3) For the Tune Power -4.5 dB carrier level (adjustable with R148), control signal uP19, "Coupler Tune", is logic low, turning on PIN diode CR19. With CR19 turned on, resistor R147 is effectively placed in parallel with R152, reducing the carrier level. Tune Power is selected when the 100/500 Watt Antenna Coupler is in a tune sequence. The reduced carrier level yields a sufficient amount of RF power for tuning.

r. 455 KHz IF Amplifiers Q6/Q7. Transistors Q6/Q7 form a feedback pair, with the 455 KHz IF level for the mixer appearing at the Q7 emitter and a higher 455 KHz IF level for the ALC circuit appearing at the Q7 collector. The resultant 455 KHz is divided by precision resistor pad/divider R158/R159 and applied to mixer M1.

s. Local Oscillator (LO) Amplifier/Switch Q15. The 40 MHz LO input to mixer M1 is via amplifier/switch Q15. The purpose of the switch function is to completely disable mixer M1 during periods of reception. This is accomplished by using the control signal "+15V-T", which is +15V only during transmit. The +15V-T turns on transistor Q15 and the LO signal is amplified and applied to M1-8 only during transmit.

t. TGC Control CR29/CR30. Transmitter Gain Control (TGC) action is via PIN diodes CR29/CR30. The TGC control voltage enters the exciter board via J5-6 and is applied to a fast attack/slow decay time constant formed by R186-R188/C103/CR28. The TGC voltage varies the resistance of the PIN diodes and the desired attenuation characteristic is obtained. A complete description of the overall 100 Watt Transceiver TGC action is provided in the description for AGC/TGC Board A1A6.

u. 40 MHz IF Amplifier Q17/Q18. The 40.455 MHz IF is amplified by transistor feedback pair Q17/Q18. As in the case for 40 MHz LO switch Q15, 40.455 MHz IF amplifier Q17 is operated by the control voltage +15V-T. Therefore, the transistor pair is active only during periods of transmission.

v. 40 MHz IF BIT Detector Q19/Q20/Q28. During the BIT testing sequence, a 1 KHz audio tone is injected for modulation. The 40.455 MHz IF is sampled and fed to amplifiers Q28 and Q19. The resultant 40.455 MHz IF is rectified by diodes CR31/CR32. The dc voltage from the rectifiers is filtered and applied to switch Q20, which turns on. A +dc input to Q20 causes uP100, "40 MHz TX IF Modulation Detector" output, to go to logic 0.

w. 455 KHz ALC Feedback Signal AR12A,B.

(1) The 455 KHz IF level from Q7 is envelope detected by diode CR17 with a 9V peak signal output. The adjacent components, including diode CR16, are used for temperature compensation. The CR17 detected output is filtered and applied to voltage follower AR12A-3. The output of AR12A-1 exits the exciter board at J5-1 to the AGC/TGC Board as the "455 KHz IF Envelope Out". Another AR12A-1 signal path is routed to voltage comparator AR12B-5.

(2) AR12B-6 has a 9V threshold set by R170-R172. When the envelope input to AR12B-5 is higher or lower than the threshold, the output AR12B-7 switches between +15V and -15V, respectively. When a peak is detected and the output of AR12B is high, transistor Q9 is turned on, forming a fast charging current for capacitor C93. The voltage on C93 turns on transistor pair Q10/Q11, which turns on PIN diode CR15, thereby reducing the peak signal to an acceptable level. The voltage on C93 discharges through R174 and R185 in parallel, unless Q13 is off, in which case C93 discharges only through R174.

x. ALC Time Constant Select Q12/Q13/Q14.

(1) To prevent the ALC circuit from tracking low frequency modulation envelopes common in AME, the ALC time constant formed by C93/R174 is very long. However, to allow a faster acting circuit in modes other than AME, the C93/R185 time constant is desired.

(2) The 455 KHz IF envelope from AR12A-1 is applied to voltage comparator AR13A. A threshold reference is established at AR13A-2 by resistors R177 and R178 in parallel with R179, and is equal to +1.6 V. The voltage source for the divided reference is +10.000V.

(3) When a signal exceeds the selected threshold at AR13A, the output of AR13A goes to +15V and transistor Q12 is turned on. While Q12 is on, a charging current is supplied to capacitor C94.

When C94 has charged to +5 Vdc, the output of voltage comparator AR13B-7 switches to -15 Vdc and transistor Q13 is turned off. With transistor Q13 off, the C93 time constant is between C93 and R174. In the CW mode, control signal uP0, "CW Audio/Keyline Select", turns on transistor Q13, regardless of the AR13A output, and the C93 time constant is always short because R174 and R185 are placed in parallel.

y. VOX/ANTI-VOX Keyline U6.

(1) A transmit audio input sample is used to automatically generate a keyline when audio is detected. This is the Voice Operated Transmit (VOX) function. The sampled audio comes from one of three sources: MIC, AUD2 or PATCH. When operating from any of these three audio inputs, the VOX feature can be enabled. To prevent keying of the 100 Watt Transceiver during receive operations, a sample of the receive audio is used to generate an ANTI-VOX signal that is combined with the VOX signal. Both the VOX and ANTI-VOX samples have adjustable thresholds to permit the operator to compensate for a variety of operating conditions.

(2) Device U6A is a voltage controlled amplifier for the VOX audio sample. The VOX variable gain control adjustment is located on the front panel of the 100 Watt Transceiver (VOX). The front panel control is adjusted by the operator to set the threshold level of VOX action to compensate for high background noise, low voice input levels, etc. The audio signal at the output of U6A is rectified by CR4/CR5 and filtered by C26. The resulting +dc is applied to Operational Amplifier AR4B-3.

(3) Device U6B is a voltage controlled amplifier for the ANTI-VOX audio sample. The ANTI-VOX variable gain control adjustment is located on the front panel of the 100 Watt Transceiver (ANTIVOX). The control is positioned by the operator to set the threshold level to prevent unintentional VOX operation during periods of receiving. The audio signal at the output of U6B is rectified by CR6/CR7 and filtered by C32. The resulting -dc is applied to Operational Amplifier AR4B-3 to reduce the +dc VOX level by the desired amount.

z. Operational Amplifier AR4B. AR4B is configured as a summing amplifier and voltage comparator to compare the VOX dc input and a voltage reference. The +100 millivolt reference established at AR4B-2 is applied via precision voltage divider R65/R66. When the VOX input is above the +100 mV reference, the comparator has a high output (keyed, +15V); when the VOX input is below the reference, the comparator has a low output (unkeyed, -15 V). Resistor R64 provides feedback from the output to the non-inverting input and adds a small amount of hysteresis to assure complete switching. The AR4-1 output is applied via isolation diode CR8 to AR5-2.

aa. CW Key Switch U1, Q30, Q1. The CW key switch consists of three 2-input NAND gates, U1, and transistors Q30 and Q1. U1A is an inverting buffer for the transceiver CW keyline. The output of U1A, along with the CW AUDIO SELECT signal from the microprocessor, is fed into U1C. If both these inputs are high (indicating that CW mode is selected on the transceiver front panel and the transceiver CW key is activated), the output of U1C is a low, which is then applied to one input of U1B. U1B functions as an OR gate, outputting a high if either or both of its inputs is low. The other input to U1B is the CW keyline from the Remote Control Unit, which is active low. Therefore, if either CW keyline is activated, U1B outputs a high, which turns on transistor Q30. If Q30 turns on, it causes Q1 to turn on, which sends a high to pin 2 of VOX/CW Keyline Comparator AR5. When keyed in CW, the output of Q1 is +15 Vdc; when unkeyed, the output of Q1 is 0 Vdc.

ab. Keyline Delay Select U8.

(1) The VOX and CW keylines are combined at the input to AR5-2 and applied to capacitor C34, resistor R287, and resistors selected by transistor array U8. When keyed, the combined VOX/CW line is at +15 Vdc and capacitor C34 is charged. When VOX/CW is unkeyed, the input to AR5-2 remains at +15 Vdc until C34 can discharge. AR5 is a Field Effect Transistor (FET) device with an extremely high input impedance; therefore, C34 can only discharge via parallel resistors.

(2) The "hang time" for the VOX/CW keyline, developed by C34, is determined by the parallel resistor R287 plus the resistor selected by U8. The purpose of the keyline "hang time" is to allow faster sequential keying of the 100 Watt Transceiver rather than have each key closure start a keyline sequence from the beginning. This assures CW and voice segments will not be clipped during transmissions.

(3) U8 is a transistor array in a Darlington configuration where the resistors connected to the device are effectively grounded when a control signal is applied. When the control signal uP0, "CW

Audio/Keyline Select", is applied, resistors R68/R69 are in parallel with R287. Since R68 is a variable resistor, 10 to 510K ohms, the "hang time" is adjustable from 0.100 to 3 seconds. Control signal uP8, "VOX Voice Delay Select", allows a "hang time" adjustment with R70 from 0.15 to 3 seconds. Control signal uP9, "VOX Data Delay", inserts a fixed resistor R71, and the "hang time" is fixed at 0.04 seconds.

(4) U8 control signal uP12, "TX Inhibit", uses two portions of U8 to maintain the proper sense of the control signal, and inserts a fixed resistor R295, resulting in a "hang time" of 0.04 seconds. "TX Inhibit" is used to remove any charge from C34 to assure the 100 Watt Transceiver will not power up in a keyed condition.

ac. VOX Keyline Comparator AR5.

(1) The inverting input to FET Operational Amplifier AR5-2 is the combined VOX/CW keyline. The AR5-3 input is a +2.6 V reference voltage, derived from the voltage divider formed by R72/R73. When the +15 V keyline input at AR5-2 is decaying via C34 and the selected parallel resistor, the output of AR5-6 remains low until the +15 V keyline has decayed to the reference level of +2.6 V.

(2) When the keyline has decayed to +2.6 V, the output of AR5-6 switches from -15 V to +15 V and the 100 Watt Transceiver unkeys. Resistor R74 provides feedback from the output to the non-inverting input to insert a small amount of hysteresis that assures complete switching. During rapid keying in VOX and CW operations, C34 is constantly "updated" with +15 V and the voltage at AR5-2 does not decay to the +2.6 V reference level until the adjusted "hang time" has expired.

(3) The output of AR5-6 is -15 V when VOX/CW is keyed and +15 V when VOX/CW is unkeyed. Diode CR9 clamps the -15 V circuit output to -0.7 V (keyed). Resistors R75/R76/R77 form a 3-to-1 voltage divider, reducing the +15 V circuit output to +5 V (unkeyed).

ad. Keyline Switching U11/U13.

(1) A 100 Watt Transceiver keyline is developed from one of the following keyline inputs:

VOX/CW Key	Generated on the Exciter Board.
PTT Key	Push-to-Talk input from handheld microphone.
AUD2 PTT Key	Audio 2 input keyline.
EXT Key	External Key from terminals at rear of 100 Watt Transceiver.
AFSK Key	Audio Frequency Shift Key input.
uP Self Key	Keyline entered at 100 Watt Transceiver front panel. Used to generate a local keyline and for automatic keying in tuning the 100/500 Watt Antenna Coupler.

(2) All input keylines, except for AFSK and uP Self Key, are buffered by AND gate U27. Buffering is followed by switching for all keylines except uP Self Key and EXT key. The uP Self Key is from the control board and is switched prior to application to this board. The EXT key is not switched, in order to allow this input to override any of the selected keylines. In the CW mode, if EXT key is used, the CW "hang time" becomes infinite, with the CW key still keying the output carrier on and off. The switching commands are generated from the Exciter Board MCB bus registers.

ae. Keyline Debounce U14. All input keylines, except uP Self Key, are combined and applied to U14B-13 Inverter/Schmidt Trigger. This shapes the keyline into a fast rising key strobe and is further shaped and inverted by U14A. Keyline debounce is provided by driver transistor Q21 and RC time constant R220/C114. The processed keyline is then applied to PROM U15.

af. PROM Keyline Decode U15.

(1) A number of discrete components are eliminated by the use of PROM U15. The inputs to U15 include;

Switched Keyline	The summation of the debounced keylines
TX inhibit	uP12 input (prevents 100 Watt Transceiver keying while changing frequencies, or during time when 100/500

Watt Antenna Coupler elements are returning to "home" for a retune cycle)

TX RF mute — Logic input that allows a keyline but mutes output RF.

uP Self key — Local keyline available to operator at 100 Watt Transceiver front panel, or for automatic keying such as used in 100/500 Watt Antenna Coupler operations.

+15V-T/R — A PROM output signal processed and routed back to PROM input. Provides timing for transmit/receive switching.

(2) The other PROM input is grounded. The bit map for PROM U15 is shown in Table 5-3. The input conditions (256 possibilities) yield a unique 4-bit output at terminals O1-O4.

(3) The outputs of U15 PROM are designated;

O1 — "Raw Key"
Routed to the A1A12 Control Board. Used to illuminate front panel XMIT indicator and other control board functions.

O2 — "Conditioned Key"
Routed to other 100 Watt Transceiver modules, including T/R relay, and also used on the Exciter Board to indicate a keyed condition.

O3 — "+15V-T/R"
Used for switching the +15V source to create +15V-T (+15V only during transmit) and +15V-R (+15V only during receive) outputs.

O4 — "Carrier Enable"
Used for switching, for Exciter Board functions, for AME carrier injection and for partial carrier 100/500 Watt Antenna Coupler tune cycles.

(4) The output keylines occur in sequence to prevent hot switching of relays. The order of the sequencing for a key down condition is: "Conditioned Key" followed by "+15V-T/R", followed by "Carrier Enable". At release of key, the sequencing is: "+15-T/R" simultaneously with "Carrier Enable", followed by "Conditioned Key". These three PROM outputs are buffered and inverted by transistors Q23-Q25.

ag. +15V-T/R Conditioning AR10A.

(1) Portions of the 100 Watt Transceiver are active in the receive mode only or in the transmit mode only but not in both modes. To prevent interaction difficulties, these portions are powered with +15 V only during their respective operations. This requires the generation of +15V- T (+15V only in transmit) and +15V-R (+15V only in receive). The control for the +15V-T/R switching is conditioned by AR10A comparator.

(2) The input for AR10A-6 is a +1.6V reference from precision voltage divider R228/R229. This is compared with input AR10A-5 which is the +15V-T/R control signal after slow attack/fast decay processing. The slow attack characteristic is provided by R226/C115 and fast decay by CR42/R289/C115. The fast decay is enabled when the output of PROM U15.switches from transmit (logic 0) to receive (logic 1). In fast decay, transistor Q24 is turned on, grounding the cathode of CR42. The charge of C115 is then quickly drained and the potential at AR10A-5 falls below the AR10A-6 reference, with the output AR10A-7 switching to -15V. Diode CR33 blocks the -15 V, hence, the output to devices U16A,C is approximately 0 V.

Table 5-3.

BIT MAP FOR MEMORY DECODE PROM U15

Code is listed in hexadecimal format:

Binary	Hexadecimal (Hex)
0000	0
0001	1
0010	2
0011	3

Binary	Hexadecimal (Hex)
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B

Binary	Hexadecimal (Hex)
1100	C
1101	D
1110	E
1111	F

The bit map Hex is decoded for the address (AD) and data (DA) information. An example is shown below:

AD	DA		Address (AD)								Data (DA)			
			A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1
2C	D	===>	0	0	1	0	1	1	0	0	1	1	0	1
			[	2		]	[	C		]	[	D		]

PROM format is 256x4 where an 8-bit input address (A0-A7) identifies one of the 256 4-bit outputs (O1-O4).

AD	DA	AD	DA	AD	DA	AD	DA	AD	DA	AD	DA	AD	DA	AD	DA
00	A	10	A	20	A	30	2	40	B	50	B	60	B	70	3
01	A	11	A	21	A	31	2	41	A	51	A	61	A	71	2
02	B	12	B	22	B	32	3	42	B	52	B	62	B	72	3
03	B	13	B	23	B	33	3	43	A	53	A	63	A	73	2
04	A	14	A	24	A	34	2	44	B	54	B	64	B	74	3
05	A	15	A	25	A	35	2	45	A	55	A	65	A	75	2
06	B	16	B	26	B	36	3	46	B	56	B	66	B	76	3
07	B	17	B	27	B	37	3	47	A	57	A	67	A	77	2
08	C	18	C	28	E	38	E	48	D	58	D	68	F	78	F
09	C	19	C	29	E	39	E	49	C	59	C	69	E	79	E
0A	D	1A	D	2A	F	3A	F	4A	D	5A	D	6A	F	7A	F
0B	D	1B	D	2B	F	3B	F	4B	C	5B	C	6B	E	7B	E
0C	C	1	C	2C	E	3C	E	4C	D	5C	D	6C	F	7C	F
0D	A	1D	A	2D	A	3D	2	4D	A	5D	A	6D	A	7D	2
0E	D	1E	D	2E	F	3E	F	4E	D	5E	D	6E	F	7E	F
0F	B	F	B	2F	B	3F	3	4F	A	5F	A	6F	A	7F	2
80	0	90	0	A0	0	B0	0	C0	0	D0	0	E0	0	F0	0
81	0	91	0	A1	0	B1	0	C1	0	D1	0	E1	0	F1	0
82	0	92	0	A2	0	B2	0	C2	0	D2	0	E2	0	F2	0
83	0	93	0	A3	0	B3	0	C3	0	D3	0	E3	0	F3	0
84	0	94	0	A4	0	B4	0	C4	0	D4	0	E4	0	F4	0
85	0	95	0	A5	0	B	0	C5	0	D5	0	E5	0	F5	0
86	0	96	0	A6	0	B6	0	C6	0	D6	0	E6	0	F6	0
87	0	97	0	A7	0	B7	0	C7	0	D7	0	E7	0	F7	0
88	0	98	0	A8	0	B8	0	C8	0	D8	0	E8	0	F8	0
89	0	99	0	A9	0	B9	0	C9	0	D9	0	E9	0	F9	0
8A	0	9A	0	AA	0	BA	0	CA	0	DA	0	EA	0	FA	0
8B	0	9B	0	AB	0	BB	0	CB	0	DB	0	EB	0	FB	0
8C	0	9C	0	AC	0	BC	0	CC	0	DC	0	EC	0	FC	0
8D	0	9D	0	AD	0	BD	0	CD	0	DD	0	ED	0	FD	0
8E	0	9E	0	AE	0	BE	0	CE	0	DE	0	EE	0	FE	0
8F	0	9F	0	AF	0	BF	0	CF	0	DF	0	EF	0	FF	0

(3) Slow attack is enabled when the output of PROM U15 switches from receive (logic 1) to transmit (logic 0). In slow attack, transistor Q24 is turned off and capacitor C115 charges via resistor R223/R226. When the voltage on C115 equals the AR10-6 reference, the output of AR10-7 switches to +15V. Resistor R227 provides a small amount of hysteresis feedback for complete switching.

ah. +15V-T/R Switching Q26/Q27. The processed +15V-T/R control signal is used to alternately switch on transistor Q26 or Q27. Inverters U16A,B double invert so that the "receive" logic low is applied to the base of Q27, turning on the transistor. With the transistor on, +15V is routed to the +15V-R line through current limiting resistor R240. The "transmit" logic high is inverted by U16C to logic low, turning on transistor Q26. With the transistor on, +15V is routed to the +15V-T line through current limiting resistor R235.

ai. Exciter Module Control Bus (MCB) Interface. The MCB originates on the A1A12 Control Board and interconnects all microprocessor controlled RF modules. A description of MCB operation is provided in the A1A12 Control Board paragraphs.

aj. MCB Decode U19.

(1) The MCB address, AD0-AD3, is decoded by 1-of-8 decoder U19. The exciter board decoder U19 is shared with the AGC/TGC board; therefore, U19 decodes two MCB addresses. The Exciter Board address is "5" (logic 0101) (ADD3=0, ADD2=1, ADD1=0, ADD0=1) and the AGC/TGC address is "9" (logic 1001) (ADD3=1, ADD2=0, ADD1=0, ADD0=1).

(2) The Q2 and Q4 outputs of decoder U19 are inverted by U20E,F to develop the correct logic sense. The developed outputs are fast "strobes" rather than sustained logic signals, and include "Exciter-Write", "Exciter-Read", and "AGC/TGC-Write". Note that an "AGC/TGC-Read" is not required since the "read" function from the AGC/TGC module is combined with the exciter readback (see description for shift register U25).

ak. Bus Registers U21, U22, U23, U24.

(1) Serial data inputs consist of 4 bytes (32 bits). The data stream is clocked into bus registers U21-U24 with exactly (32) 625 KHz clock pulses. Once the data is clocked into the registers, the MCB address and "write" commands are received. The data in the U21-U24 shift registers are then latched into the U21-U24 storage registers and appear at the bus register Q outputs in parallel. This cycle is conducted by the control board to update and reconfigure the Q outputs as demanded by user and CPU commands.

(2) Each output of U21-U24 serves a function, typically, to operate a solid-state switch. The Exciter Board functions are given an "uP" designation, e.g., uP7 = 1 KHz Audio Select, uP10 = PTT Select, etc. The U21-U24 outputs not associated with the exciter board include "CW/AFSK" (with driver/inverter Q29), low pass filter commands for "Bypass", "Band Select" and "Bite Enable", and a "Loop Back" that is used as part of the exciter BIT testing. The uP commands are discussed in the circuit where they are active, and the LPF commands are discussed in the A1A5 Low Pass Filter paragraphs.

(3) The "Loop Back" bit is the first to enter the bus registers when the 32 exciter bits are clocked in, and ends up in the last position in U24 (Q8). This bit is read back to the control board as part of the BIT "loop back" testing sequence. If the control board does not verify the position of this bit during BIT, then an Exciter MCB fault is suspected, or the Exciter Board is missing from the 100 Watt Transceiver.

al. Shift Register U25. Readbacks to the control board from the exciter are the inputs to shift register U25. In addition to the exciter "Test Out" input discussed above, there are two additional exciter board BIT inputs as well as Low Pass Filter, Power Amplifier, and TGC BIT inputs. During exciter BIT sequencing, a 1 KHz Tone is injected into the audio path and used to modulate the 455 KHz carrier, which in turn is up-converted to 40.455 MHz. At two points in the circuit, the 455 KHz and 40.455 MHz signals are envelope detected. For a properly operating circuit, a signal is detected at each point and converted into a dc signal, i.e., the U25 inputs "455 KHz MOD BIT" and "40 MHz MOD BIT". The remaining BIT inputs are generated on other assemblies and are discussed in their respective paragraphs. The U25 enable is from the "Exciter-Read" strobe generated in Decoder U19 as discussed above. The same strobe is used to enable tri-state inverter U20C,D. The parallel inputs to U25 are clocked out in serial with the "clock" signal input.

am. Clock Buffers U20. The input "clock" signal is buffered by tri-state inverters U20A,B. The U20 enable is grounded for a permanent "enable". In

addition to isolating the clock source, the buffers reduce the loading on the control board clock.

an. Enable U14. To prevent random data from appearing at bus registers U21-U24 during power up, the U21-U24 "enable" lines are not initialized until the +5 Vdc input power stabilizes. The +5 V input charges capacitor C135 via R280. After approximately 400 milliseconds, the output of U14D goes to logic low, which in turn causes the output of U14E to go to logic high. The logic high output of U14E is used as the U21-U24 "enable". When the 100 Watt Transceiver is turned off, capacitor C135 is discharged through R279/CR43.

ao. TGC Interface J10-29,19,22. The decoding for the AGC/TGC module is accomplished on the Exciter Board as discussed for device U19. Only the data "write" function is used, since the "read" is accomplished with a BIT input to shift register U25. The AGC/TGC interface consists of the "AGC/TGC-Write" strobe, the 625 KHz "clock", and the MCB serial data port. Operation of the TGC interface is discussed under AGC/TGC Assembly A1A6.

ap. +10.000 V Reference U26. The +15 V is applied to three terminal precision voltage reference U26 to generate a very accurate +10.000 V. The +10.000 V is used as a reference for the exciter ALC (Automatic Level Control) and TGC (Transmitter Gain Control) circuits. The current draw for U26 is 5 milliamperes. Capacitors C100 and C101 at the input/output terminals are used for decoupling.

aq. VSWR Meter Select U17A,B. The 100 Watt Transceiver front panel displays of forward power, reverse power, and VSWR are selected by the VSWR Meter Select circuit, using solid state switches U17A and U17B. The RF output levels of the 100 Watt Transceiver or Linear Power Amplifier (LPA) are sampled by their respective discriminator circuits, which yields an analog representation of the forward and reflected RF output levels. When the 100 Watt Transceiver is operating without an LPA, the XCVR path is selected; when operating with an LPA, the LPA path is selected, using Exciter Board control bit uP16. The selected signals are divided by voltage dividers R247/R248 and R259/R260 and routed to the control board A1A12, where they are converted from analog signals to digital signals. The digital signals are processed by the microprocessor to illuminate the correct meter segments for Forward Power and Reverse Power. In addition, the digital word is processed in software for the front panel VSWR display.

ar. Power Supply Decoupling C117-C125, L16-L18. The capacitor/inductor components C117-C126 and L16-L18 at the +15 V, -15 V, and +5 V inputs remove spurious RF signals from the voltage source lines. Since a number of RF signals are present on the exciter board, the decoupling components are used primarily to prevent signals from escaping the exciter board rather than to prevent signals from entering the assembly.

as. Low Power Indicator AR11A.

(1) The low power indicator circuit is used to illuminate a front panel LOW PWR indicator when the transmitted RF output level from the 100 Watt Transceiver/LPA falls below an adjustable threshold. The "Conditioned Key" input via CR38 and R250 ensures that the circuit is operational only during periods of transmission.

(2) The VFWD forward power analog voltage, selected by the VSWR Meter Select circuit, is sampled by R249 and CR36. When transmitting, the keyline is at low potential, effectively placing R252 in parallel with capacitor C126. This results in a fast attack (via R249/CR36) and slow decay (via R252) characteristic for the sampled VFWD. Therefore, when pauses occur in voice transmissions, the LOW PWR indicator will not illuminate unless the decay time of 5 seconds elapses.

(3) The sampled voltage is compared with a reference voltage in AR11A. When the sampled voltage falls below the reference, the output of AR11A goes positive (+15 V), which is reduced to a nominal +5 V by resistor R258 and zener diode VR2 (4.7 V). Therefore, the output at J7-31 is +5 V for a low power condition.

(4) The LOW PWR threshold is adjustable from 0 dB to -6 dB. This allows a range of operating conditions where the 100 Watt Transceiver can be operating at lower power levels and the LOW PWR indicator can be adjusted accordingly.

5-18 IF FILTER PWB ASSEMBLY, A1A2, 10085-5300. This manual portion describes the IF Filter PWB as an individual assembly. Section I of this chapter describes the function of the IF Filter PWB in relation to overall 100 Watt Transceiver operation.

The following references apply for the detailed discussion that follows:

a. Schematic Diagram	Depot Manual
b. Parts List	Depot Manual
c. Component Layout	Depot Manual
d. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
e. Overall Interconnection	Figures FO-11,FO-12
f. Transceiver Assembly Schematic Diagrams	Depot Manual

5-19. OVERALL IF FILTER P W B FUNCTION. The 455 KHz IF is amplified and filtered on the IF Filter assembly. The assembly is used during both transmitting and receiving operations.

a. IF Filter frequencies. Three standard 455 KHz IF filters are selectable, plus three additional filters for the AFSK mode, with the following frequencies of operation:

(1) LSB Filter 455.350-458.050 KHz

(2) USB/AME Filter 451.950-454.650 KHz

(3) CW Filter 454.800-455.200 KHz

(4) AFSK, ± 42.5 Hz 454.945-455.055 KHz

(5) AFSK, ± 85 Hz 454.890-455.110 KHz

(6) AFSK, ± 425 Hz 454.450-455.550 KHz

b. IF Filters vs frequency scheme. The frequency scheme of the 100 Watt Transceiver reverses the sidebands, hence, the USB filter operates below 455 KHz and the LSB filter operates above 455 KHz. Since the AME mode is USB (reduced 6 dB) plus carrier (reduced 6 dB), the USB and AME modes use the same filter. The CW filter is centered at the 455 KHz IF frequency as are the AFSK filters. In CW and AFSK modes, the 1st LO injection frequency is offset to convert inputs to a 455 KHz 2nd IF center frequency.

c. IF Filter selection control. Filter selection is accomplished by Module Control Bus (MCB) commands. The MCB provides two select control signals and an enable signal. The MCB interface is located on Receiver PWB A1A7, with the control signals routed to the IF Filter assembly via Interconnect PWB A1A15. Filter selection is accomplished by diode switching circuits. The BIT signal developed on the IF Filter assembly is also routed to the Receiver PWB, forming part of a readback word to Control Board A1A12. Additional information regarding the MCB interface for the standard IF Filters will be found in the discussion on the Receiver Assembly, and for the AFSK filters in the AFSK Assembly discussion.

d. CW LSB/USB select switch. The CW LSB/USB select switch is located on the IF Filter assembly. The CW signal is audio derived, with either a USB or an LSB offset, i.e., the actual transmitted signal is either 1 KHz above (USB) or below (LSB) the front panel frequency display. For example, if the USB switch position is selected, and the 100 Watt Transceiver operating frequency is 10.000 000 MHz, then the actual transmitted frequency is 10.001 000 MHz. The switch setting is read back to the control board along with the IF Filter BIT via the MCB interface on the Receiver PWB.

5-20. DETAILED IF FILTER BOARD CIRCUIT DESCRIPTION. The paragraphs below provide detailed circuit descriptions of the IF Filter assembly. Each description heading begins with a device number, e.g., Q1, Q2, etc., identifying the circuit under discussion. The detailed information follows the signal flow shown on IF Filter Board schematic diagram. The detailed information assumes the overall IF Filter assembly function is understood from the simplified descriptions provided in earlier paragraphs.

a. Filter Decoder U1A. The MCB input control signals are applied to U1A which decodes the two select lines to generate a single (1 of 4) output. When the U1A enable signal is logic low, the input select lines A and B select one of the four Q outputs. The selected Q output goes to logic high, and the unselected Q outputs go to logic low. When the U1A enable signal is at logic high, the input select lines A and B have no effect and all Q outputs go to logic low. The control logic selects one of the filter paths based on the following truth table:

Select Select (CW) (USB/AME) (LSB) (Not Used)

B	A	Q3	Q2	Q1	Q0
0	0	0	0	0	1

B	A	Q3	Q2	Q1	Q0
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Enable = 0
(Enable = 1, all Q outputs = 0)

b. Filter Driver/Selector AR1, AR2. The non-inverting inputs (+) for AR1/AR2 are connected to a fixed reference of +2 V. The inverting input (-) is connected to the outputs of the U1A filter decoder. When a filter is selected, the AR1/AR2 (-) input is +5 Vdc and the output of the voltage comparator is -15 Vdc. The -15 volt signal turns on the diodes in the selected signal path. The ground return path is via resistors R10 and R33. The other AR1/AR2 voltage comparator outputs are +15 Vdc, which turns on shunt diodes for the unselected signal paths and reverse bias the respective series diodes.

c. Filter selection example. For example, if the USB filter is selected, the output of U1A-Q2 is +5 Vdc. This causes the output of AR1A to switch to -15 Vdc, while all other voltage comparator outputs are at +15 Vdc. Diodes CR9/CR12 are forward biased and turned on. With the diodes turned on, the 455 KHz IF signal follows this low resistance path and the circuit is completed. Diodes CR10/CR11 are reverse biased and present a high resistance path to the IF signal. Diodes associated with all other filters prevent signals from passing through these filters.

d. Input amplifier Q1, Q2, Q3. The unfiltered 455 KHz IF input is amplified by transistors Q1 and Q2. The gain of the Q2 stage is adjusted by R5. Transistor Q3 is configured as an emitter follower output for impedance matching to the filter input circuit. The processed 455 KHz IF is then routed to the selected filter, as discussed above.

e. Output amplifier Q4, Q5. The filtered 455 KHz IF is buffered by feedback transistor pair Q4 and Q5. The low impedance output at the Q5 emitter is AC-coupled to a voltage divider consisting of R38 and R39, which provides a 50 ohm output impedance at connector J2. The 455 KHz IF output is sampled by C29 and applied to a BIT detector circuit.

f. BIT detector Q6, Q7, Q8. The 455 KHz IF sample is amplified by two- stage amplifier Q6 and Q7. The output of Q7 is rectified by CR18/CR19 to generate a +dc voltage whenever the 455 KHz IF is detected. The +dc level turns on transistor Q8 and causes the BIT output to be logic low. During BIT sequencing, all three filters are tested.

5-21. FIRST CONVERTER PWB ASSEMBLY A1A3, 10085-5000. This manual portion describes the First Converter PWB as an individual assembly. Section I of this chapter describes the function of the First Converter PWB in relation to overall 100 Watt Transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram	Figure 5-4
b. Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
f. Overall Interconnection	Figures FO-11,FO-12
g. Transceiver Assembly Schematic Diagrams	Depot Manual

5-22. OVERALL FIRST CONVERTER PWB FUNCTION. The First Converter PWB has a bi-directional function and is used in both receive and transmit operations. In receive operation, it converts a received signal between 1.600,000 and 29.999,990 MHz to an IF frequency of 40.455 MHz. In transmit operation, it converts a 40.455 MHz transmit IF signal to a final transmit RF frequency between 1.600,000 and 29.999,990 MHz. Extensive use is made of +15V-T (+15 Vdc only during "transmit") and +15V-R (+15 Vdc only during "receive") as control signals to configure the PWB for each of the signal paths. The injection local oscillator (LO) signal originates at Synthesizer PWB A1A10 and ranges from 42.055 to 70.45499 MHz. The desired mix in receive is LO - RF = 40.455 MHz. For example, if an operating frequency of 12.345,670 MHz is displayed at the transceiver front panel in a voice mode (USB, LSB, AME), then the LO injection frequency is 52.800,670 MHz (52.800,670 - 12.345,670 = 40.455 MHz).

5-23. DETAILED FIRST CONVERTER BOARD CIRCUIT DESCRIPTION. The paragraphs below provide detailed descriptions of the First Converter PWB assembly circuits. Each description heading contains a device designator,

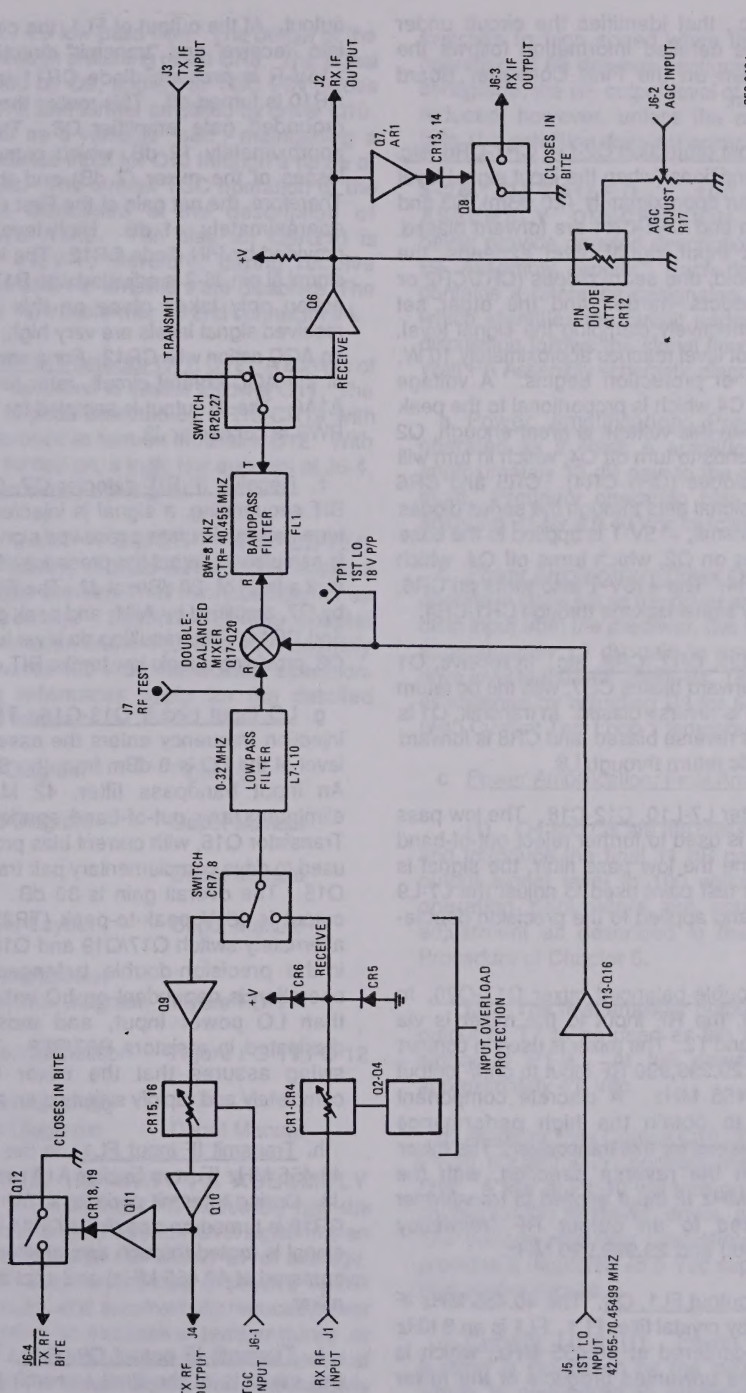


Figure 5-4. Simplified Diagram, First Converter PWB

e.g., Q1,Q2, etc., that identifies the circuit under discussion. The detailed information follows the signal flow shown on the First Converter Board schematic diagram.

a. Receiver input protection Q2-Q4, CR1-CR6, etc. Under normal conditions (when the input signal level is no stronger than approximately +20 dBm), Q3 and Q4 are turned on and CR1-CR4 are forward biased. When the peak input signal level exceeds the protection threshold, one set of diodes (CR1/CR2 or CR3/CR4) conducts harder and the other set conducts less, effectively clamping the signal level. When the RF input level reaches approximately 10 W, a second stage of protection begins. A voltage develops across C4 which is proportional to the peak signal level. When this voltage is great enough, Q2 turns on, which tends to turn off Q4, which in turn will turn off all four diodes (CR1-CR4). CR5 and CR6 clamp whatever signal gets through the series diodes CR1-CR4. In transmit, +15V-T is applied to the base of Q2. This turns on Q2, which turns off Q4, which turns off CR1-CR4. The +15V-T also turns on CR6, which clamps any signal leakage through CR1-CR4.

b. T/R switch Q1, CR7, CR8, etc. In receive, Q1 turns on, which forward biases CR7, with the dc return through L6. CR8 is reverse biased. In transmit, Q1 is turned off, CR7 is reverse biased, and CR8 is forward biased, with the dc return through L6.

c. Low pass filter L7-L10, C12-C18. The low pass filter (0-32 MHz) is used to further reject out-of-band signals. Following the low pass filter, the signal is sampled at J7 (a test point used to adjust the L7-L9 filter elements), and applied to the precision double-balanced mixer.

d. Precision double-balanced mixer Q17-Q20. In the receive path, the RF input to the mixer is via transformers T1 and T2. The mixer is used to convert the 1.600,000 to 29.999,990 RF input to an IF output centered at 40.455 MHz. A discrete component mixer is used to obtain the high performance characteristics desired for this transceiver. The mixer also operates in the reverse direction, with the transmit 40.455 MHz IF input applied to transformer T3 and converted to an output RF frequency between 1.600,000 and 29.999,990 MHz.

e. Receive IF output FL1, Q6. The 40.455 MHz IF output is filtered by crystal filter FL1. FL1 is an 8 KHz bandpass filter centered at 40.455 MHz, which is used to reject the unwanted products of the mixer output. At the output of FL1, the circuit path divides into "receive" and "transmit" directions. In receive, +15V-R is present, diode CR11 is turned on, and CR10 is turned off. This routes the output of FL1 to grounded gate amplifier Q6. The gain of Q6 is approximately 12 dB, which compensates for the losses of the mixer (7 dB) and the filters (4 dB). Therefore, the net gain of the First Converter PWB is approximately +1 dB. High level AGC control is provided by PIN diode CR12. The input AGC control signal at pin J6-2 is adjusted with R17. However, AGC action only takes place on this assembly when received signal levels are very high; typically, there is no AGC action with CR12. For a complete description of the AGC control circuit, refer to AGC/TGC PWB A1A6. The IF output is sampled for BIT and exits the PWB at connector J2.

f. Receive IF BIT detector Q7, Q8, AR1. During BIT sequencing, a signal is injected at the antenna terminals to simulate a received signal. The receive IF is sampled to detect the presence of the BIT IF which is at a level of -20 dBm at J2. The IF signal is buffered by Q7, amplified by AR1, and peak detected by CR13 and CR14. The resulting dc level turns on transistor Q8, providing a logic low for the BIT output at J6-3.

g. LO input circuit Q13-Q16. The First LO input injection frequency enters the assembly at J5. The level of the LO is 0 dBm from the Synthesizer PWB. An input bandpass filter, 42 MHz to 70 MHz, eliminates any out-of-band spurious frequencies. Transistor Q16, with current bias provided by Q13, is used to drive complementary pair transistors Q14 and Q15. The overall gain is 30 dB. The LO voltage output is 18 V peak-to-peak (TP2) and is used to alternately switch Q17/Q19 and Q18/Q20 transistors in the precision-double balanced mixer. Mixer operation is dependent on LO voltage swing rather than LO power input, and most LO power is dissipated in resistors R67/R68. The high voltage swing assures that the mixer transistors are completely and rapidly switched on and off.

h. Transmit IF input FL1. In the transmit mode, a 40.455 MHz IF from Exciter A1A1 enters the PWB at J3. During transmit periods, +15V-T is active, diode CR10 is turned on and diode CR11 is turned off. The signal is routed through crystal filter FL1 (8 KHz BW, centered at 40.455 MHz) and applied to the precision mixer.

i. Transmit IF output Q9, Q10. The RF output of the mixer is at the final transmit frequency and is

routed to the L7-L9 low pass filter. The output of the filter passes through switching diode CR8. The signal is then amplified by Q9, applied to TGC PIN diodes CR15 and CR16, and further amplified by driver Q10. The diodes act as a variable "pad", maintaining a constant impedance input for Q10 through a range of control voltages. The overall TGC operation of the transceiver is discussed in the description of AGC/TGC PWB A1A6. The bias for Q9/Q10 is derived from +15V-T; therefore, during receive periods, the transmit RF amplifiers are disabled. The signal output is via transformer T6 and connector J4.

j. Transmit RF BIT detector Q11, Q12. A sample of the transmit RF is routed to emitter follower Q11. The output of Q11 is peak detected by CR18/CR19 with the resulting dc used to turn on transistor Q12. With transistor Q12 turned on, a logic low appears at J6-4, indicating the presence of a signal.

5-24. 100 WATT POWER AMPLIFIER ASSEMBLY A1A4, 10085-8010. This manual portion describes the 100 Watt PA Assembly as an individual assembly. Section I of this chapter describes the function of the 100 Watt PA Assembly in relation to overall 100 Watt Transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram	Figure 5-5
b. Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
f. Overall Interconnection	Figure FO-11,FO-12
g. Transceiver Assembly Schematic Diagrams	Depot Manual

5-25. OVERALL 100 WATT PA ASSEMBLY FUNCTION. The 100 Watt PA Assembly has the primary function of amplifying a low level signal into an output RF power signal of 100 watts PEP or average. The 100 Watt PA is protected from excessive VSWR levels, short circuits, and automatically reduces power output if operating at excessive temperatures or current levels. A cooling fan operates at low speed at normal 100 Watt PA temperatures, and automatically switches to high speed when the 100 Watt PA is operating at 65 degrees centigrade. At 95 degrees centigrade, the RF output level of the 100 Watt PA is reduced; however, unless the cooling fan system fails, this condition does not occur during regular use.

5-26. DETAILED 100 WATT PA ASSEMBLY DESCRIPTION. The paragraphs below provide detailed descriptions of the 100 Watt PA Assembly circuits. Each description heading contains a reference designator, e.g., Q1, Q2, etc., which identifies the circuit under discussion. The discussion follows the signal flow shown on the 100 Watt PA Assembly schematic diagram.

a. Power Amplification: Predriver Q1. Q1 is operated as a class A amplifier and introduces approximately 13 dB gain to the nominal +13.5 dBm input. Predriver operating bias is established by adjusting R1 for a 0.40 Vdc indication at TP3.

b. Power Amplification: Driver Q2, Q3. Q2 and Q3 operate in class AB as the driver amplifier. With +26.5 dBm input from the predriver, this stage will introduce approximately 13 dB gain to provide a +39.5 dBm drive level to the final amplifiers. Driver amplifier bias is established by adjusting R3 for 517 mV across R66 (with Current Test Loop 1 temporarily removed).

c. Power Amplification: Final Amplifier Q4, Q5.

(1) Q4 and Q5 are the class AB final amplifiers, and introduce the final 11 dB gain to increase the output signal level to 100 watts. Final amplifier operating parameters are established by bias adjustment as described in the Bias Adjustment Procedure of Chapter 6.

(2) The final amplifier output is sampled at the output of T7 to be used as the PA TX BIT output signal at P1-9. At full power, the voltage is approximately 4.0 Vdc.

d. Amplifier Bias Control Q10, VR1. The voltage at P1-10 (COND KEY) controls the bias of transistor Q10. A low at P1-10 will turn on Q10 to effect bias control for the predriver, driver, and final amplifiers. The voltage regulator consisting of Q10 and VR1 provides a regulated +5.5 Vdc supply for all amplifier bias control circuits.

e. Current Limit U1. Power Amplifier current loading is monitored by the current sense circuit, which is configured to produce a current sense

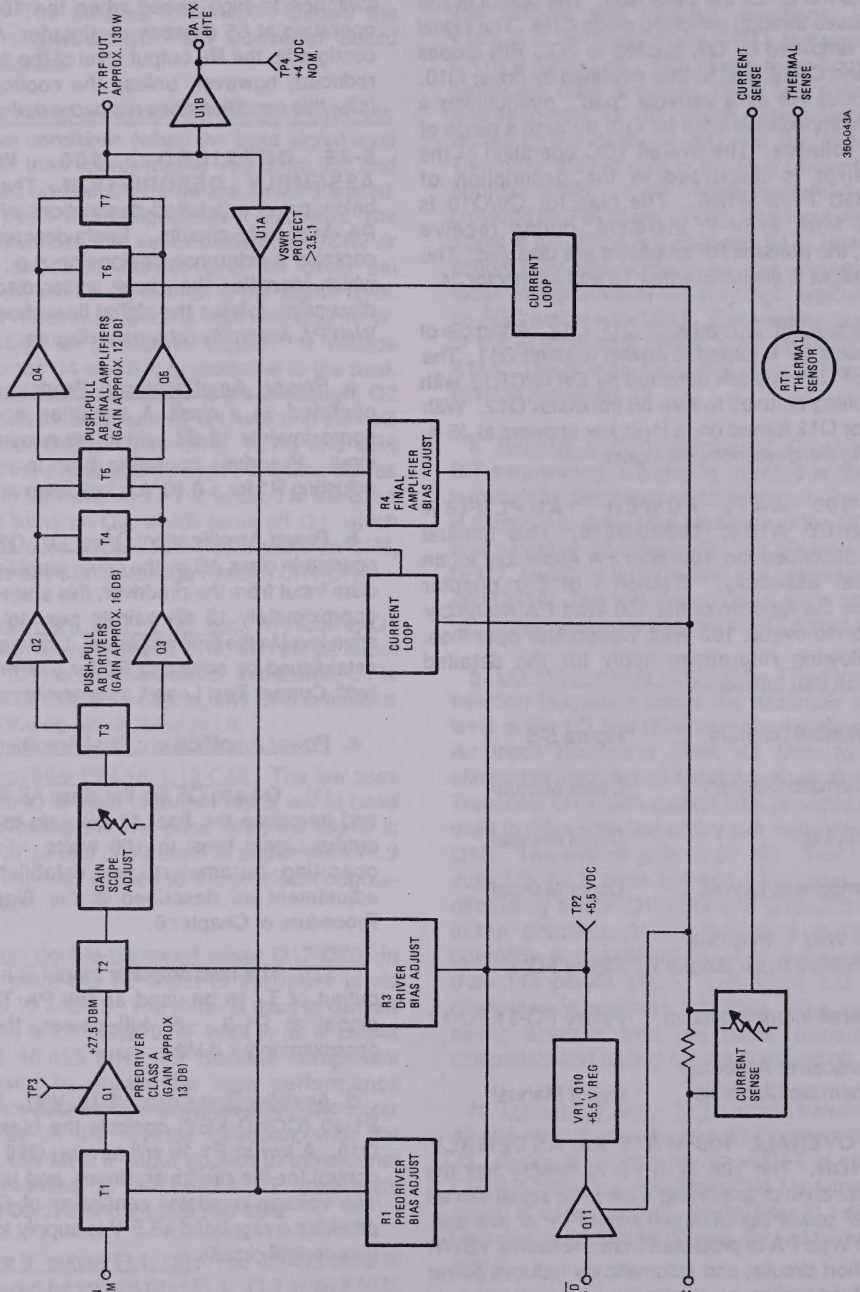


Figure 5-5. Simplified 100 Watt PA Assembly

output proportional to the voltage drop across R61 through R64. R61 through R64 are in series with the +13.2 Vdc supply line to the PA. The sense output level can be adjusted by R5. R5 is adjusted so that current cutback action will start with a 120 mV drop across R61 through R64.

f. Thermal Sense RT1. RT1 is mounted to the PA heatsink to monitor PA operating temperature. The resistance of RT1 is nominally 119 K ohms. This resistance changes as a function of temperature so that at 105 degrees centigrade the resistance drops to 5K ohms (the point at which power cutback starts). If the temperature increases to 115 degrees centigrade, the resistance of RT1 drops to 3.6 K ohms. The thermal sense output voltage then causes the transmitter to shut down.

5-27. LOW PASS FILTER PWB ASSEMBLY A1A5, 10085-4000. This manual portion describes the Low Pass Filter PWB as an individual assembly. Section I of this chapter describes the function of the Low Pass Filter PWB in relation to overall 100 Watt Transceiver operation. The following references apply for the detailed discussion that follows:

a Schematic Diagram	Depot Manual
b. Parts List	Depot Manual
c. Component Layout	Depot Manual
d. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
e. Overall Interconnection	Figures FO-11,FO-12
f. Transceiver Assembly Schematic Diagrams	Depot Manual

5-28. OVERALL LOW PASS FILTER PWB FUNCTION. The purpose of the Low Pass Filter (LPF) PWB is to provide harmonic and out-of-band frequency filtering for the receive and transmit RF signals with a series of six 7-pole elliptical low pass filters. The 1.600,000 to 29.999,990 MHz operating range of the 100 Watt Transceiver is divided into six bands of operation:

a. Band 1 1.600,000 to 2.599,990 MHz
b. Band 2 2.600,000 to 4.199,990 MHz
c. Band 3 4.200,000 to 6.799,990 MHz
d. Band 4 6.800,000 to 10.999,990 MHz
e. Band 5 11.000,000 to 17.999,990 MHz
f. Band 6 18.000,000 to 29.999,990 MHz

a. Filter Selection. Band selection for a low pass filter is determined by the operating frequency of the 100 Watt Transceiver. For example, an operating frequency of 12.345,670 MHz selects the band 5 low pass filter. Note that the filters themselves are low pass, not band pass; e.g., the selection of band 5 selects a low pass filter that operates from dc to 17.999,990 MHz. The primary function of the filter is to remove harmonics of the transmit frequency. The band selection control signals are routed to the Low Pass Filter PWB from the Module Control Bus (MCB) interface on Exciter PWB A1A1. Also included is a "BIT Enable" logic line, and a readback "LPF BIT" logic line.

b. BIT feature. During BIT sequencing, the "BIT Enable" signal is true during portions of the receive BIT of the 100 Watt Transceiver. This injects an output from an oscillator operating at 2.4576 MHz into the receive RF path, which simulates a received signal at -18 dBm.

c. Output power sample. Also located on the LPF is a directional coupler which develops "XCVR Vrefl" and "XCVR Vfwd" voltage levels that are used in controlling output power via the transmitter gain control (TGC) circuit and also provide for front panel display of forward and reflected power.

5-29. DETAILED LOW PASS FILTER BOARD CIRCUIT DESCRIPTIONS. The paragraphs below provide detailed descriptions of the Low Pass Filter assembly circuits. The detailed information follows the signal flow shown on the Low Pass Filter Board schematic diagram.

5-30. TRANSMIT SIGNAL PATH.

a. T/R Relay. The J1 RF input to the LPF is at a 100 watt level, PEP or average, which comes from 100W PA Assembly A1A4. When the keyline is closed, the "Conditioned Key" input at J5-6 is logic low and transistor Q1 is turned on. With transistor Q1 turned on, "Transmit/Receive" (T/R) relay K13 operates and the "transmit" path is selected.

b. Filter Selection.

(1) The 100 Watt Transceiver operating frequency automatically selects one of the six low pass filters. The input control logic for band selection

is applied to relay driver/inverter U1. The selected filter control line is +5 Vdc; the unselected control lines are 0 V. The selected U1 driver/inverter output is at ground potential which closes a pair of relays at the input/output of a low pass filter, and the transmit RF passes through the filter. The portions of the LPF that are not selected are grounded by the select relays to minimize stray RF pickup.

(2) The transmit RF passes through a directional 100 watt coupler/discriminator assembly, another low pass filter, and exits the assembly via J2. The J2 output is connected directly to the 100 Watt Transceiver rear panel RF INPUT/OUTPUT connector J1.

c. Discriminator.

(1) The discriminator samples the transmit RF voltage, via capacitor C187, and the transmit RF current, via transformer T1, to determine the parameters of the antenna load impedance. The desired impedance is 50 ohms resistive. The T1 current sample balance is adjusted with control R18, i.e., the junction of R15/R16 and R18/R36 will "see" the ends of T1 as being 180 degrees out of phase with each other. The discriminator voltage and current samples are rectified and combined to form dc analog voltages representative of the transmit RF forward and reflected power levels. For example, if the transmitter RF antenna load is the desired 50 ohms resitive, the processed voltage and current samples (phase and level) will add for Vfwd and cancel for Vrefl.

(2) A non-resitive load results in a phase shift between the current and voltage samples. Any load other than 50 ohms results in a level shift between the current and voltage samples. The net results are the Vfwd/Vrefl output parameters that are routed to the A1A6 AGC/TGC PWB to control the power output levels of the 100 Watt Transceiver, and routed to the A1A12 Control PWB to develop front panel meter power displays during transmission. The output of the discriminator for a 100 watt, 50 ohm condition is +8 Vdc.

d. RF Sample. A high impedance voltage divider, consisting of R13, R14 and R34, samples the output RF level and routes it to LPF J4, and then to the 100 Watt Transceiver rear panel connector, RF SAMPLE J2. The RF sample level is 70 dB below the transmit RF output power level (uncalibrated). When operating at full power, the transmitter output is 100 watts (+50 dBm); therefore, the sample output is 0.01 milliwatt (-20 dBm) into 50 ohms. The output level at a nominal -20 dBm allows direct connection to spectrum analyzers, voltmeters, etc.

e. Thermal Protection. A thermistor sensor RT1 detects excessive LPF operating temperatures. RT1 forms a part of a voltage divider with R19, R20 and R21. The thermistor has a negative temperature coefficient of 4%/degree C; therefore, as RT1 heats, the "cold" resistance of 50K ohms begins to decrease. As RT1 decreases in resistance, the output of the voltage divider decreases from a "cold" value of +10 Vdc to a "hot" value of -3 Vdc. The divider voltage output is amplified X2 by AR2 (non-inverting), forming the J5-11 "thermal" output. The LPF "thermal" output is monitored by the A1A6 AGC/TGC PWB where the TGC circuit will reduce output RF power if an excessive LPF temperature is detected.

f. RFI Reduction. To prevent high RF transmit voltages from appearing throughout the 100 Watt Transceiver, decoupling is used at all input and output power and control lines. In addition, the +13.6 V used to operate the LPF selection relays is further decoupled into +13.6V-A and +13.6V-B segments.

5-31. RECEIVE SIGNAL PATH.

a. Input Circuit. Signals received at the antenna are routed to the 41.5 MHz low pass filter (L20, L21) to reduce any large out-of-band components. The input is then routed through one of six low pass filter segments (selected as previously discussed). Following filtering, the received signal is routed to the T/R relay.

b. Transient Protection. To prevent damage to the transceiver in the case of transient voltages, surge protector E1 is placed across the input terminals at J2. If an excessive voltage appears at J2, device E1 "breaks down", shorting the voltage to ground. After the surge passes, E1 "recovers" and continues its protection.

c. T/R Relay. When operating as a receiver, the relay contacts are in the relaxed (receive) position. The keyline input "Conditioned Key" is not grounded; therefore, transistor Q1 is not turned on, and T/R relay is not operated. The received signal then exits the LPF via connector J3 for application to 1st Converter Assembly A1A3.

5-32. LOW PASS FILTER BIT FUNCTIONS.

a. Low Pass Filter BIT Oscillator. During BIT sequencing for verification of the 100 Watt Transceiver receive signal path, a simulated antenna input is generated by oscillator Y1/Q2. The oscillator is enabled by logic input "BIT Enable", and has an output of 2.4576 MHz at a level of - 18 dBm (level is adjustable using R1, and frequency is adjustable using C1). The enable signal also activates relay K14, placing the relay in the "Test" position.

b. Low Pass Filter BIT Detector. The BIT detector consists of amplifiers Q5 and AR1. The simulated receive input is buffered by Q5 and amplified by AR1, and applied to peak detector diodes CR1/CR2. The rectified output turns on transistor Q4, placing a logic low on output terminal J5-12, "LPF BIT". Input protect diodes prevent damage to the BIT detector circuitry when high input signals are received during normal operations.

c. BIT Sequencing. During low pass filter BIT testing, no LPF segment is initially selected. This condition is verified by the control board by observing the absence of a logic low at terminal J5-12. The purpose of this step is to verify that no LPF RELAY is "stuck" in the closed position. Next, the filters are sequenced from band 1 through band 6. Since all filters are low pass, the test oscillator signal of 2.4576 MHz passes through all filters and is detected in sequence. (The assignment of frequency "bands" is used only to identify which filter is selected for each 100 Watt Transceiver operating frequency.) After the LPF passes BIT, the band 6 filter is selected, and the BIT 2.4576 MHz test oscillator signal continues to function, generating the test signal for subsequent module testing.

5-33. AGC/TGC PWB ASSEMBLY A1A6, 10085-5250. This manual portion describes the AGC/TGC PWB as an individual assembly. Section I of this chapter describes the function of the AGC/TGC PWB in relation to overall transceiver operation. The AGC and TGC portions of the board operate independantly of each other and are discussed separately. The following references apply for the detailed discussion that follows:

a. Simplified Diagram - AGC	Figure 5-6
b. Simplified Diagram - TGC	Figure 5-7
c. Simplified TGC Detector Operation	Figure 5-8
d. Schematic Diagram	Depot Manual
e. Parts List	Depot Manual
f. Component Layout	Depot Manual
g. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
h. Overall Interconnection	Figures FO-11,FO-12
i. Transceiver Assembly Schematic Diagrams	Depot Manual

5-34. OVERALL AGC FUNCTION.

a. AGC Detector. The purpose of the AGC portion of the AGC/TGC PWB is to provide Automatic Gain Control (AGC) during receive operation, resulting in constant audio output levels with a varying input receive signal. The AGC signal is "IF derived" from the 455 KHz IF signal via the AME envelope detector on the Receiver PWB, which is connected during all receive operations. The dc output from the AME detector is maintained at approximately +0.4 Vdc for the entire 120 dB AGC dynamic range for receive levels of -100 dBm to +20 dBm. At receive levels below -100 dBm, the receiver operates at full gain (no AGC control); at receive levels above +20 dBm, automatic protection circuits open the receive path to protect the front end circuits from damage.

b. AGC Dynamic Range. AGC action is provided at three points in the receive circuit path for the 120 dB dynamic range. The "2nd IF AGC" output (0 to -12 Vdc) has a 60 dB dynamic range; the "1st IF AGC" output (-6 Vdc to +6 Vdc) has a 40 dB dynamic range; and the "RF AGC" output (0 to -12 Vdc) has a 20 dB range. The AGC outputs do not always operate simultaneously. For received signal strengths of -100 dBm to -80 dBm, only the "2nd IF AGC" is operating. For received strengths from -80 to 0 dBm, both the "2nd IF AGC" and "1st IF AGC" are operating. For signal strengths from 0 dBm to +20 dBm, all three AGC outputs are operating. Over the dynamic range of the AGC, the maximum output audio variation does not exceed 6 dB. AGC action starts at about 10 dB above receiver sensitivity, with a Signal+Noise/Noise ratio of 20 dB.

c. AGC Loop Operation. The AGC circuit forms a loop so that the detected 455 KHz IF signal always

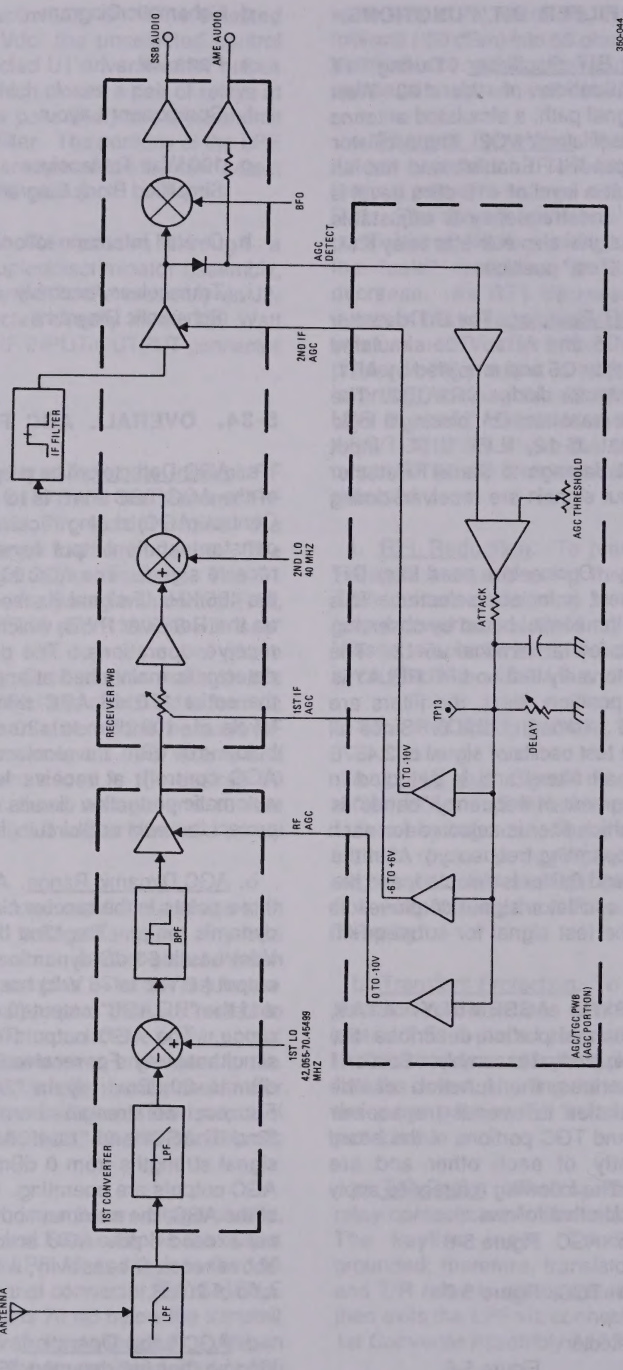


Figure 5-6. Transceiver Simplified AGC Diagram

yields a constant voltage at full audio output. This dc output is compared with a threshold reference at the AGC board. If the detected output is below or above the threshold, AGC action adjusts the gain of the receiver to make them equal. For example, if the received signal level decreases and the detected output drops below +0.25 Vdc, the AGC responds by increasing the gain of the receiver (more signal to detect) until the detected signal is again nominal. If the received signal increases and the detected output rises above +0.4 Vdc, then the AGC responds by decreasing the gain of the receiver (less signal to detect) until the detected signal is again nominal.

d. AGC Speed. The speed with which the AGC "attacks" a change in signal level is fixed at less than 30 milliseconds (maximum) for a 30 dB step in signal input. The speed with which AGC "decays" after a signal change is selectable: "Fast", "Medium", or "Slow". For example, in SSB voice operations, pauses in speech result in no received signal. With a "fast" AGC decay characteristic, an immediate rise in speaker noise would occur as the gain of the receiver rapidly increased to compensate for the lack of signal. With a "slow" decay, the AGC present during voice operations is maintained during breaks in speech patterns and the receive gain is thus kept constant. The selectable AGC speeds are:

(1) AGC: FAST 30 milliseconds decay time

(2) AGC: MED 200 milliseconds decay time

(3) AGC: SLOW 4 seconds decay time

e. AGC OFF. In addition to selecting an AGC speed, the operator may select AGC OFF. This mode disables all normal AGC action and the gain of the receiver is controlled by the front panel RF GAIN control. The AGC OFF mode is selected when normal AGC action is not optimal for the listening conditions.

f. Manual AGC Control. The transceiver front panel RF GAIN control can be used to manually control the gain of the transceiver. When the RF GAIN control is turned counterclockwise from its normal full clockwise position, the RF GAIN will override the normal AGC action and manually adjust the gain of the receiver. The RF GAIN control can be used with any AGC speed, or in the AGC OFF mode. If used in the AGC OFF mode, the RF GAIN control has complete control over the receiver gain and there is no AGC action of any kind.

g. Meter Vsig Output. A monitoring of the AGC level gives an indication of the received signal strength. The AGC voltage, before passing through shaping networks for the three AGC control outputs, has a linear 12 dB/volt (0 to +10 Vdc) characteristic. This is buffered to generate "Vsig" and applied to the A1A12 Control PWB for application to the front panel meter display. A processed output also appears at the rear of the transceiver on TB1-5, AGC TEST, for external monitoring of the receiver signal strength.

5-35. DETAILED AGC CIRCUIT DESCRIPTION. The paragraphs below provide detailed descriptions of the AGC circuits. Each description heading begins with a reference designator, e.g., Q1, Q2, etc., which identifies the exact circuit under discussion. The detailed information follows the signal flow shown on the AGC/TGC PWB schematic diagram.

a. AR16 AGC Detector Amplifiers.

(1) The detected 455 KHz IF sample is routed from the Receiver PWB to J1-29 as the input AGC signal. For a full audio signal, the voltage is a nominal +0.4 Vdc. The detected dc is amplified and inverted by AR16A and applied to inverter/amplifier AR16B. Amplifier AR16B has its non-inverting (+) input connected to AGC THRESHOLD adjustment R167. If the detected and amplified AGC signal output of AR16A is below the AR16B threshold voltage, the output of AR16B saturates at -15 Vdc, and no AGC control voltage is generated. Below the threshold level, the received signal is too weak to generate an AGC control voltage. When the detected AGC signal is at, or above, the AR16B threshold voltage, an AGC control voltage is developed.

(2) AGC THRESHOLD R167 is adjusted so that a received signal of -103 dBm just starts AGC action. This is indicated by a 0 Vdc level at the output of AR16B, as measured at TP11. As the received signal level increases, the voltage increases linearly at 12 dB/volt. Therefore, for the 120 dB dynamic AGC range of the transceiver, the voltage at TP11 ranges from 0 Vdc (-100 dBm received signal) to +10 Vdc (+20 dBm received signal).

b. AR17 - AR20 AGC Speed Select.

(1) The 0-10 Vdc AGC control voltage generated at the output of AR16B (TP11) is buffered by FET amplifier AR17, which is in a non-inverting voltage-follower configuration. Diode CR42 prevents

a negative AGC output when the received level is below AGC threshold. The AGC developed at this point is now manipulated with a time constant network to shape the AGC action into a "fast attack" and adjustable "decay" characteristic. The timing capacitor, C59, is a precision low-leakage, non-polarized, component that charges quickly during AGC attack through R168 (and R183 for large signal steps) and discharges through R168 and the selected AGC speed resistors: R169 or R170, and R171.

(2) The AGC decay speed select logic is developed from the MCB interface on the A1A7 Receiver PWB, and routed via the A1A15 Interconnect PWB to the AGC circuit. When J1-28 AGC FAST goes to logic high (+5 Vdc), voltage comparator AR18A output swings from -15 Vdc to +15 Vdc and transistor Q17 turns on. This places resistor R169 in series with R168 and the time constant for the discharge of C59 is set by these resistors. AGC MEDIUM operation is similar, with AR18B and Q18/R170 setting the decay characteristic. If neither AGC FAST nor AGC MED is selected, then transistors Q17 and Q18 are both turned off. This leaves R171 as the only discharge path, and it sets the AGC SLOW time constant.

(3) The decay selection resistors, R169-R171, are connected to a -12 Vdc source, instead of ground, to linearize the discharge of C59. Capacitor C59 is prevented from holding a negative charge by diode CR43. The processed AGC is then amplified by FET voltage-follower amplifier AR20. The use of high impedance FET amplifiers assures that C59 discharges only through the selected "decay" resistors. Measurements of AGC voltage at TP12 will affect the AGC "attack" and "decay" characteristics since the input impedance of the test equipment will alter the impedance across C59.

c. Q24 AGC Disable. If the operator selects the AGC OFF mode, a logic high at J1-31, "AGC Disable", turns on transistor Q24. This places a ground on the AGC line via R217, and the AGC output drops to 0 Vdc. R217 prevents damage to Q24 by current limiting the rapid discharge of C59. A control signal, "AGC Dump", at J1-30, also turns on Q24 to discharge C59; however, the "AGC Dump" feature is not used during normal operation.

d. AR22-AR25 AGC Output. The processed AGC appearing at test point TP13 ranges from 0 to +10 Vdc. Measurement at TP13 gives a direct indication of the received signal strength as follows:

Processed AGC	Received Signal Level	
TP13	dBm	Volts (rms into 50 ohms)
0V	-100 dBm	2.23 uV
+1V	-88 dBm	8.88 uV
+2V	-76 dBm	35.34 uV
+3V	-64 dBm	140.7 uV
+4V	-52 dBm	560.1 uV
+5V	-40 dBm	2.23 mV
+6V	-28 dBm	8.88 mV
+7V	-16 dBm	35.34 mV
+8V	-4 dBm	140.7 mV
+9V	+8 dBm	560.1 mV
+10V	+20 dBm	2.23 V

The 0-10V AGC developed at TP13 is applied to a number of input and output circuits. Diodes CR44, CR47, CR48 and CR57, form an "OR" function and the more positive input assumes control of the AGC line. The diodes also block the negative outputs from any of the connected operational amplifiers.

e. External AGC Input. The "External AGC" input at J1-27, via AR25A, may override the normal AGC function. However, this input is not used in current configurations.

f. RF Gain Input. The "RF Gain" input is derived from the front panel RF GAIN control and is used to override normal AGC action, or to establish the receiver gain in the AGC OFF mode. The RF GAIN voltage follower AR22A is used with diode CR48 to assure that only the positive output is applied to the AGC line.

g. +15V-Transmit Input. The receiver circuits are automatically placed in the low gain configuration during transmit by overriding the 0-10V AGC line with a +15V-T input.

h. Vsig Output. The 0-10V AGC voltage at TP13 is a linear indication of received signal strength. It is routed to the A1A12 Control PWB, for the front panel "S" meter display.

i. 2nd IF AGC Output. The 0-10V AGC voltage is applied to the shaping network components associated with devices AR21A and AR23A. The shaping network is required to compensate for the

non-linear characteristics of the PIN diode attenuators that control the AGC amplifiers. Compensation is the reverse of the PIN diode characteristic to obtain an overall linear response and is in the form of three straight line approximations. The 2nd IF AGC output from AR23A-1 is used until the AGC voltage at TP13 exceeds the threshold of AR21A-2 at which time a different characteristic is developed. Emitter follower Q21 provides a low impedance output for the final 2nd IF AGC.

j. 1st IF AGC Output. The 1st IF AGC has a shaping network similar to that of the 2nd IF AGC, except that two straight line approximations are made to linearize the overall 1st IF AGC response. In addition, the 1st IF AGC is not active until the received signal strength is above -80 dBm. This requires each of the operational amplifiers to have a threshold setting derived from the -15V source. As AGC voltage rises, the various operational amplifiers are enabled in sequence to generate the desired overall AGC response.

k. RF AGC Output. The RF AGC output does not require an elaborate shaping network. However, the RF AGC threshold requires a received signal strength of 0 dBm for the circuit to become active. This threshold is set by precision resistors R210 and R211. Driver emitter follower Q23 assures a low impedance output for the RF AGC.

5-36. OVERALL TGC FUNCTION. The TGC circuit is shown in simplified form in figure 5-7. The purpose of the Transmitter Gain Control (TGC) portion of the AGC/TGC PWB is to conrol the PEP or average output power at a level of 100 watts. The circuit operates as a control loop whose elements are a voltage comparator, a digital-to-analog converter, and a group of PIN diode attenuator circuits. When the comparator determines that the RF output power is too high or too low, a digital counter is incremented or decremented. The 8 bits from the digital counter are applied to a digital-to-analog converter, yielding a dc voltage which changes the attenuation of the PIN diodes to increase or decrease the RF output power accordingly. The generated TGC voltage is a slower acting average power control, combined with a faster acting Peak Power Control (PPC). TGC is applied as the steady long-term control voltage, where the PPC injects control to immediately reduce excessive RF power peaks. The PPC operates via a threshold detector, and when active, is coupled directly to the TGC output.

5-37. TGC OPERATION. The primary task of the TGC circuit is to compare a highly stable 455 KHz IF envelope with a detected RF output envelope. The TGC circuit maintains these envelopes at a constant ratio following all positive and negative peaks of the impressed modulation. When the ratio is above or below the desired ratio, the RF power level is adjusted. The comparison of the IF and RF envelopes is accomplished in the TGC voltage comparator. The comparator has a negative output if the RF output power is excessive, a positive output if the RF output power is insufficient, and zero output if the RF output power is correct. The circuit also establishes a "dead zone" that allows small variations in RF power output without power correction commands.

a. Source of TGC voltages. The RF envelope is derived from the VSWR bridge at the RF output terminal of the transceiver, and if used, an RF envelope is also derived from a Linear Power Amplifier (LPA). TGC will operate on whichever is the greater of the two envelopes. The transceiver RF envelope passes through a Voltage Controlled Amplifier (VCA) that can increase its level. The increased envelope is seen by the voltage comparator as an increased power level, and the comparator reduces the RF output level in response. There are four inputs to the VCA control that can be used to reduce the RF output power levels.

(1) Vcc Sense. A comparator circuit monitors the level of the power amplifier supply line. This is used primarily when the 100 Watt Transceiver is operating directly from a battery supply source. As the battery source begins to discharge below a threshold level (+11.0 Vdc for CW/AFSK modes and +11.3 Vdc for voice modes, as sensed at the AGC/TGC Board), the RF output power is reduced. This power reduction allows lower-distortion transmissions at low battery levels. Note that on the Vcc sense line there is also an overvoltage sense circuit (VR1/Q29). This does not have an input to the VCA, but will force a TGC reset if Vcc exceeds +17 Vdc. LED DS3 will also illuminate to indicate that Vcc is too high and that the TGC is in a "protect" mode.

(2) Low Pass Filter Temperature Sense. A thermistor sensor on Low Pass Filter Assembly A1A5 is a portion of a voltage divider between the +15 Vdc and -15 Vdc supplies. If the Low Pass Filter begins to operate at elevated temperature, the RF output power level is reduced to prevent equipment damage.

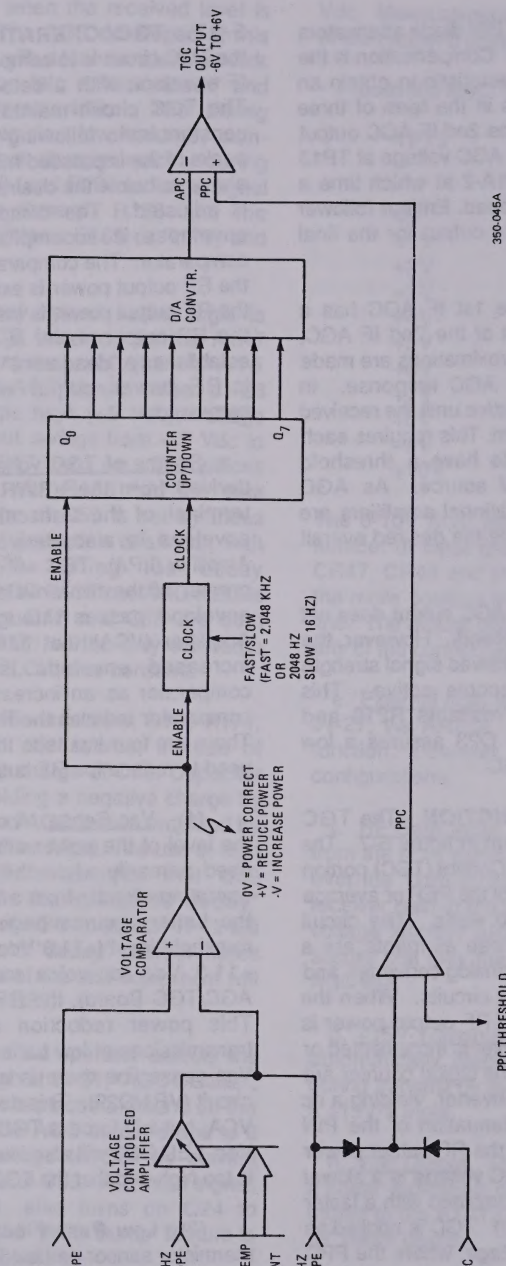


Figure 5-7. Simplified TGC Circuit Operation

(3) 100 Watt PA Module Temperature Sense. A temperature sensor on 100 Watt PA Module A1A4 can cause the RF output level to be reduced. Ordinarily, this will not occur, since the cooling fan switches to high speed well before the RF output power reduction is required and the module is maintained at an acceptable temperature level. However, should the cooling fan fail, or air passage become blocked, this sensor will prevent equipment damage by reducing the RF output level.

(4) 100 Watt PA Module Current Sense. A current sensor on 100 Watt PA module A1A4 can command the RF output level to be reduced. An excessive PA current could be an indication of equipment failure or abnormal operation. To prevent circuit damage, the RF output level is reduced when PA current becomes excessive.

b. TGC control voltage processing. When the voltage comparator has determined that a RF output power correction is required, the TGC clock is enabled. Simultaneously, an 8-bit counter (256 states) is commanded to count up or count down, depending on the polarity of the voltage comparator output. The 8 bits at the counter output are converted into a voltage by a digital-to-analog converter. At maximum count, the analog output is +10 Vdc; at minimum count, the analog output is 0 Vdc. This 0 to +10 Vdc range is converted into a -6 Vdc to +6 Vdc range for application to the PIN diodes.

5-38. TGC OPERATION - PPC. The PPC portion of the TGC signal is derived by threshold detecting the RF envelope sample. If the peak portion of the envelope exceeds the PPC detector threshold level, a control voltage is sent to the TGC circuit to reduce the output RF power level.

5-39. DETAILED TGC CIRCUIT OPERATION. For the detailed TGC circuit description discussion, refer to AGC/TGC schematic diagram.

a. TGC Input Signals. The VSWR bridge assembly on Low Pass Filter A1A5 has two outputs that are routed to the AGC/TGC PWB as inputs at terminals E1, E2, and E3. One of the inputs is an RF envelope that represents the forward output RF power (E2), and the other is an RF envelope that represents the reflected output RF power (E1). Both RF envelope inputs are buffered by amplifier AR1. Terminal E3 is chassis ground. Protection against an open (disconnected) input is provided by CR70/CR71 and associated circuit Q25/Q26. This will hold the TGC in "reset" should either line from the VSWR bridge become disconnected, thereby preventing the output power from becoming uncontrolled.

b. Power Metering Circuit. Following AR1, the RF envelopes are routed to the metering buffer amplifiers AR14A,B and drivers Q13 and Q14 to create the front panel meter inputs for the transceiver Vfwd and Vrev. The metering circuitry provides both TGC isolation and a peak-hold function; hence, the front panel meter indicates the peak power output of the transmitter. In addition to buffering, the 0 to 8 Vdc envelope signal is converted for metering to 0 to 4 Vdc.

c. Combining Forward and Reflected RF envelopes. An AR1 output is also routed, via a precision resistor network, to the input of amplifier AR4A, where the forward and reflected RF envelopes are combined into a single signal. The precision resistor values are adjusted to give greater weight to the reflected RF output envelope signal. Therefore, the reflected power signal has a greater effect per volt than the forward power signal. Diodes CR1/CR21 and R49 set a threshold level so that a reflected power signal will not make a contribution to the combined envelope signal until a VSWR of 2:1 is reached, at which time the RF output power level begins to be reduced.

d. Reduction of Reflected RF Envelope During Tune Cycle. During an antenna coupler tune sequence, when TUNE POWER REQUEST is logic low at U1-4, the reflected power RF envelope is attenuated via R11 and diode CR2. This prevents the reflected signal, normally high during an antenna coupler tune sequence, from dominating the TGC action.

e. Modification of RF Envelope for Equipment Protection. The gain of amplifier AR4A is adjusted by 100 WATT ADJUST, R37, which is the TGC adjustment for setting the transmitter at the 100 watt level. After amplification by AR4A, the combined RF envelope signal is applied to Voltage Control Amplifier (VCA) Q1/AR4B. The VCA is used to modify the RF envelope signal strength at the output of amplifier AR4B. At this point in the TGC circuit, selected factors are allowed to control the output power of the transmitter. Each factor appears at the transistor Q1, pin 7, gate as a negative dc voltage. Should the Q1, pin 7, gate go negative, the RF

envelope signal is increased at the output of AR4B, and subsequent circuits detect this as an excessive RF power output, causing the RF power output level to be reduced. The RC devices at the input to Q1, pin 7, also act as an averaging network, with resistors R41/R42 averaging the signal to prevent short peak bursts from reducing RF power output. There are four factors that can reduce the RF output power level by application of a negative voltage at Q1, pin 7:

(1) Low Pass Filter Temperature Excessive. An input from Low Pass Filter Assembly A1A5 is routed via CR66 to the input of Q1. A temperature sensing thermistor on the Low Pass Filter is part of a voltage divider between the +15 Vdc and -15 Vdc supplies. When the voltage divider yields a negative output, the RF output power is reduced. This will typically occur when the temperature is above 95° C at the Low Pass Filter.

(2) 100 Watt PA Module Temperature Excessive. If a condition exists where the 100 watt PA module rises to a high temperature, the RF output power is reduced. The THERMAL SENSE is routed via AR7A, AR2A, and diode CR4 to the input of Q1. Under normal operating conditions, a cooling fan switches to high speed and the 100 watt PA module is maintained at normal operating temperatures. However, should the fan fail, or the fan air passage become blocked, then the 100 watt PA module is protected through reduction of RF output power. The thermistor on the 100 watt PA forms a voltage divider with resistor R20 on the AGC/TGC board. As the thermistor heats up, the resistance decreases. When the threshold set at AR2A is exceeded, the output starts going negative and the RF power level is reduced. The threshold for AR2A is 95 degrees centigrade at the 100 watt PA module. A second threshold exists at comparator AR7B for the FAN CONTROL logic. At a 65 degree centigrade temperature, AR7A has a positive output, turning on transistor Q5, which places a ground on the FAN CONTROL line, and the fan switches to high speed. When the 100 watt PA module has cooled, AR7B turns off transistor Q5 and the cooling fan returns to low speed.

(3) 100 Watt PA Module Current Excessive. If the 100 watt PA module supply current rises to a high level, the RF output power is reduced. The CURRENT SENSE is routed to inverting amplifier AR2B with the output applied to Q1 via diode CR5. The threshold level of AR2B must be exceeded before there is an amplifier output. The threshold is set so that when PA supply current reaches 35 amperes, AR2B starts to have a negative output, causing the RF power level to decrease.

(4) +13.6 Vdc Supply is Low. The +13.6 Vdc supply line is monitored from the 100 watt PA module (via Vcc sense). If the voltage falls below a threshold level (+11.0 Vdc in CW/AFSK modes, or +11.3 Vdc in voice modes), the RF output power is reduced. Typically, this circuit comes into operation when the transceiver is operated from a battery supply. By reducing the RF output power, distortion of the radio signal is avoided when the battery discharges below normal voltages. The output of threshold comparator AR3A becomes negative if the +13.6 V sample drops below the threshold level. This level is applied to Q1 via CR6. Since there is a different threshold level when operating in the CW/AFSK modes, switch Q3 is turned on by a CW/AFSK logic input, changing the voltage divider input to AR3A. Thus, the threshold level is modified to suit the operating mode of the transceiver. In addition, an overvoltage condition (Vcc greater than +17 Vdc) is sensed by the VR1/Q29 circuit. If Vcc exceeds +17 Vdc, DS3 will illuminate and the TGC circuit will be placed in a reset condition.

f. PPC signal processing.

(1) The transceiver RF envelope output from AR4B is combined with the Linear Power Amplifier (LPA) output from AR5B via diodes CR13 and CR11. Therefore, if an LPA is used, either the transceiver sample or the LPA sample will have control, depending on which is at the highest level. The combined envelope signal is applied to buffer amplifier AR5A, which operates at unity gain. The output of AR5A is sampled for the PPC portion of the TGC circuit (CR20) and applied to VCA Q2/AR8A.

(2) The inputs to PPC amplifier AR6A are applied through CR20 for the transceiver and LPA RF envelopes, and through CR19 for the LPA PPC. The peak signals are weighted by a resistive network and applied to the non-inverting input of AR6A. The inverting input of AR6A is connected to a precision voltage divider. When the transceiver or LPA 0 to + 8 Vdc envelope sample exceeds +8.2 Vdc, the output of AR6A exceeds the threshold and a positive output is applied to diodes CR16/CR18 and R233. Similarly, when the LPA PPC input exceeds the AR6A threshold (approximately 5 V), a positive PPC output from AR6A is applied to CR16/CR18 and R233. The

PPC output is fast-acting to provide the rapid protection required of the TGC circuit.

(3) The positive dc CR16 output of PPC threshold comparator AR6A is inverted by AR6B to negative dc, and applied to VCA Q2 via diode CR15 and averaging network R71/R72/C13. The charge of C13 accumulates during a series of AR6B PPC outputs. A single, short PPC output adds little charge to C13; therefore, this circuit is active only when a number of PPC "hits" are detected. If C13 does charge to a negative value, the negative input to Q2 increases the gain of AR8A. This increase is seen as excessive RF output power, and the TGC circuit starts to reduce the RF output power out. Therefore, one action of the PPC circuit is to force the TGC circuit to reduce RF output power via the output of AR8A. For an explanation of fast PPC action, see q (2).

g. TGC Differential Amplifier Inputs. The output of AR8A forms the processed RF envelope input to differential amplifier AR9A inverting (-) terminal. The noninverting (+) terminal for the AR9A differential amplifier is connected to the reference 455 KHz IF envelope sample. The AR9A differential amplifier has a positive output if the RF sample is lower than the reference IF sample, and a negative output if the RF sample is higher than the reference IF sample. When the envelopes are exactly the same, the output of the AR9A differential amplifier is 0 Vdc. The comparison of the two signals is made over the entire cycle of the envelope, not just at the peak portions.

h. Voltage Comparator "Dead Zone". The 455 KHz IF envelope is also routed to AR9B which is configured as a precision diode. The output of AR9B feeds a peak hold circuit which holds the peaks of the envelope. A + 0.173 V "dead zone" level is established with an IF of 8.0 V by precision divider R95 and R97. The "dead zone" voltage is dynamic as it changes with the IF envelope signal. A "dead zone" of + 0.173 V (with an IF of 8.0 V), translates to a window of 0.2 dB, which means that at a nominal 100 watts output, power variations between 95 watts and 105 watts will not trigger a power correction cycle. The non-inverted "dead zone" signal is routed to voltage comparators AR11A and AR12A, and an inverted "dead zone" signal, generated by unity gain inverting amplifier AR10B, is applied to voltage comparators AR11B and AR12B.

i. TGC Detector. The output of AR9A is routed via R159 to AR12. Another AR9A output is routed to AR11 via low pass filter R92/R93/C15. The AR12 output is faster acting than the AR11 output, and is used as a "look ahead" enable and prevents TGC clock overshoot. The operation of the TGC detector is best shown by example, as illustrated in figure 5-8. Assuming a single tone envelope, the IF sample is +8.0 Vdc at AR9A (+). There are now three cases to consider (although device AR11 is discussed, device AR12 operates identically):

(1) Case I. When the RF sample equals the IF sample, the output of the AR9A differential amplifier is 0 volts. This is applied to the AR11 voltage comparator inputs, causing both AR11 outputs to be -15 Vdc. In this case, the RF sample falls within the "dead zone" and the clock is disabled with a 0v signal output. Since the clock is disabled, the counter command for the counter to count down is meaningless.

(2) Case II. When the RF sample is greater than the IF sample, the AR9A output is a negative voltage equal to the difference between the two samples. This voltage is compared with the "dead zone" voltage with AR11. If the differential voltage is greater than the "dead zone" voltage, as it is in this case, the output of AR11A is -15 Vdc, and the output of AR11B is +15 Vdc. The AR11B output sends a change-power command to the clock, and the clock is enabled. The AR11A output indicates that the counter should count down. Thus, the TGC detector commands a reduction in RF power.

(3) Case III. When the RF sample is less than the IF sample, the AR9A output is a positive voltage equal to the difference between the two samples. This voltage is compared with the "dead zone" voltage by AR11. If the differential voltage is greater than the "dead zone" voltage, as it is in this case, the output of AR11A is +15 Vdc, and the output of AR11B is -15 Vdc. The AR11A (+) output sends a change-power command to the clock, and the clock is enabled. The AR11A (+) output also indicates that the counter should count up. Thus, the TGC detector commands an increase in RF power.

j. IF Sample Detector. The 455 KHz IF envelope is also applied to comparator AR10A. The purpose of the comparator is to detect when the IF envelope has dropped 20 dB below a level of full output power. When this occurs, the circuit assumes a pause in the transmitted audio, or, the audio is virtually removed at the input. This means the output of AR10A is positive during normal transmit cycles, resulting in a +5 Vdc logic level after the output diode and resistor

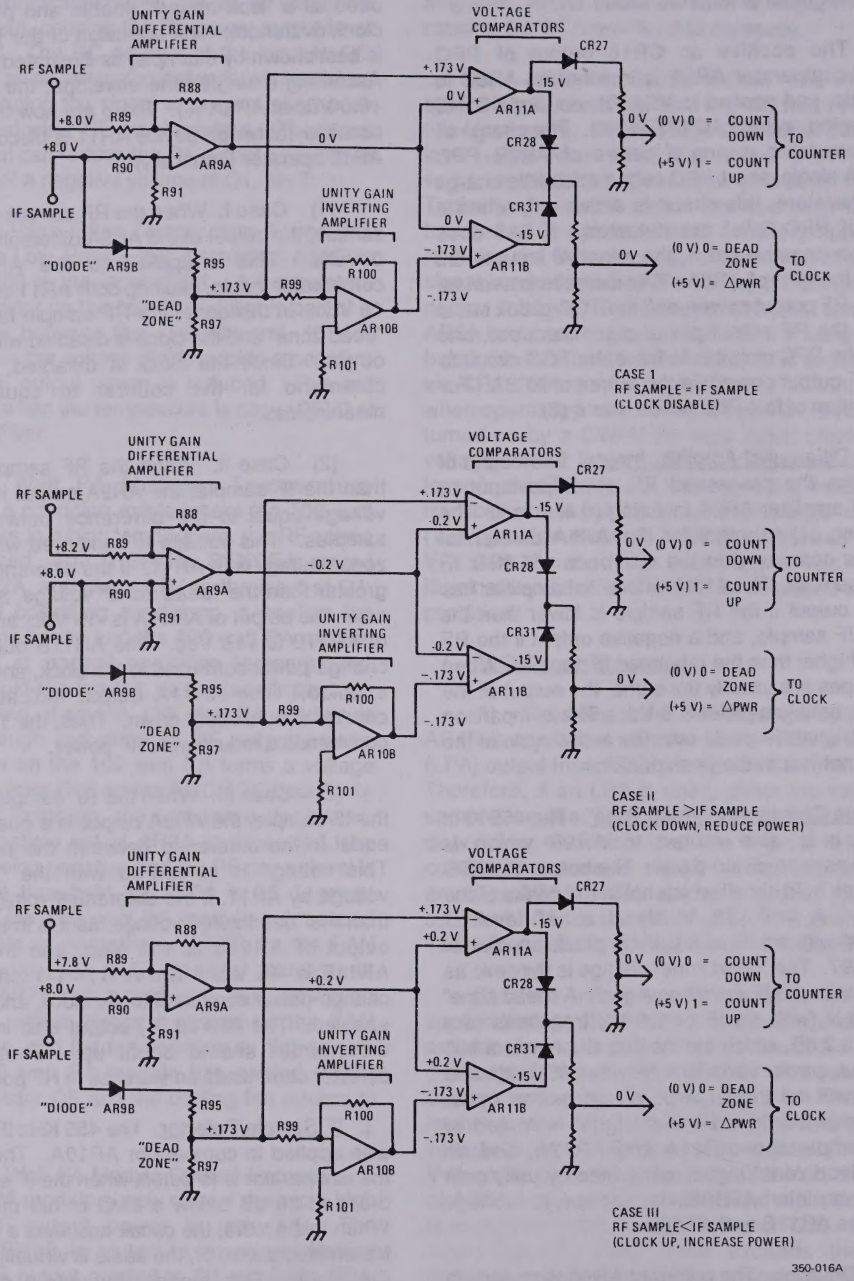


Figure 5-8. Simplified TGC Detector Operation

network. When there are no transmissions, the logic line drops to zero volts. The logic output for the IF LEVEL is routed to logic elements to "freeze" the TGC voltage, as will be discussed in subsequent paragraphs. Indicator DS2, connected to the output of AR10A, will illuminate whenever the IF envelope drops more than 20 dB below full output.

k. TGC Clock and Counter General Operation. The TGC voltage is generated by converting the contents of an 8-bit digital counter into an equivalent +dc voltage. If the counter counts up, the TGC voltage increases; if the counter counts down, the TGC voltage decreases. The TGC voltage is processed and applied to PIN diode attenuators on the Exciter and 1st Converter modules for actual RF power output control. The counter is clocked only when the clock oscillator is enabled, and the direction of the count is determined by the comparator outputs of AR11/AR12. In addition, the clocking can occur at two speeds: Slow speed for normal power control, and high speed when rapid count up or count down is required to decrease or increase power output rapidly.

l. Programmable clock selection. The U4 clock oscillator is a programmable timer with 16 ripple-binary counter stages. Counter selection is accomplished by binary code DCBA. With "B" tied to +5 Vdc, and "C" tied to ground, only "A" (pin 9) and "D" (pin 12) are under TGC logic control. The internal clock oscillator frequency, determined by external components tied to pins 3, 4 and 5, is 32,768 Hz. For TGC operation, the only logic configurations used are A = 1, D = 0, or A = 0, D = 1. (Exclusive OR U8B acts as an inverter for input "A".) For the A = 1, D = 0 mode, the logic DCBA is 0011 (divide-by-16), and a clock speed of 2048 Hz is selected. For the A = 0, D = 1 mode, the logic DCBA is 1010 (divide-by- 2048), and a clock speed of 16 Hz is selected. Therefore, references to "slow" clock refer to a speed of 16 Hz, and references to a "fast" clock refer to a speed of 2048 Hz.

m. Clock oscillator enable. The U4 clock oscillator does not have an output unless it is enabled at pin 7 with a logic low. To obtain an oscillator enable logic low, all eight inputs to NAND gates U9A/B must be at logic high. Therefore, all of the following conditions must exist to enable the TGC clock:

(1) U9A-2. RF sample is above or below IF sample, and the damping delay period has timed out. An output of AR12 is (+) dc when a power adjustment is required. This is processed by a dynamic damping circuit that adds an RC time constant delay (R114/C17). After the delay period, the input to exclusive OR gate U8A (non-iverting buffer) is logic high, placing a logic high at the U9A-2 logic input. When AR12 is (-) dc, R111 pulls the base of Q12 to ground. Q12 is then turned on by the charge stored on C17, and C17 is rapidly discharged. The damping circuit, which is derived from differential amplifier AR9A and comparators AR12A/AR12B before the delay of the low pass filter (R92/R93/C15), is a "look ahead" circuit that prevents TGC clock overshoot.

(2) U9A-3. RF sample is above or below IF sample. This is the direct input from AR12, without a damping delay. The output of AR12 is (+) dc when a power adjustment is required (via diodes and levelling resistors), placing a logic high at the U9A-3 logic input. AR12 is faster acting than AR11.

(3) U9A-4. RF sample is above or below IF sample after delay. This is the direct connection from the AR11 output (via diodes and levelling resistors), with the delay of the low pass filter R92/R93/C15. An output of AR11 is (+) when a power adjustment is required, placing a logic high at the U9A-4 input.

(4) U9A-5. The IF sample is within 20 dB of full output. This input is derived from the output of voltage comparator AR10A (previously discussed). If the IF envelope sample falls below 20 dB of the full power level, it is assumed that there is a pause in the transmitting audio input. A low IF sample level prevents clock operation, and a high IF sample (within 20 dB of full output) enables clock operation by placing a logic high at the U9A-5 input. The primary purpose of this circuit it to "freeze" the TGC voltage if there is a transmit pause, so that, at the end of the pause, the TGC action starts from the previous point rather than from zero.

(5) U9B-9. (Tied to +5 Vdc supply). This point is held logic high by connection to the +5 Vdc supply.

(6) U9B-10. LATCH command from microprocessor not present. The A1A12 Control PWB microprocessor can command the APC voltage to "freeze" at its value by generating a logic low at U1-5. If the LATCH command is not generated, a logic high is applied to U9B-10. The microprocessor control interface with the TGC circuit is described in subsequent paragraphs.

(7) U9B-11. Counter has not reached a minimum or maximum count. When the clock oscillator is enabled, the TGC counter may count to its minimum or maximum count. If a minimum or maximum count should occur, the counter has a logic low output, CARRY OUT, which is used to disable the clock oscillator. If the counter has not reached a minimum or maximum count, a logic high is applied to U9B-11 input.

(8) U9B-12. Transmitter is keyed. The CONDITIONED KEYLINE input to the AGC/TGC PWB is inverted by Q4. When the transmitter is keyed, a logic high is applied to the U9B-12 input. Between keying periods this input will have the effect of "freezing" the TGC voltage, allowing the TGC to start from the previous level rather than starting from zero.

n. Clock Speed Selection. The fast/slow clock speed command can originate from one of five sources:

(1) Microprocessor TUNE POWER REQUEST Command selects FAST clock. Fast clock is selected during TUNE POWER REQUEST (via CR8 and U1-4), which rapidly brings the transmitter to the desired power level during a tune cycle.

(2) Microprocessor FAST/SLOW Command selects either clock speed. The microprocessor can command a fast clock speed directly through the FAST/SLOW command, via CR10 and U1-14.

(3) Microprocessor RESET and PRESET RF power level commands select FAST clock. Microprocessor RESET and PRESET RF power level commands (U1-7 AND U1-6 respectively) are processed by flip-flop U7A. The U7A output Q- NOT, connected to the fast/slow clock line via CR36, can override a slow clock status and place a fast clock on the line. Q-NOT is logic low (fast clock) when a SET command is applied to U7A-6. The U7A SET command (logic high) is applied through diodes CR34 and CR35 from the U1 RESET POWER or PRESET POWER. Either of these commands causes the correct RF output power level to be acquired quickly. In the case of RESET POWER, the binary counters (U5 and U6) are directly reset to zero count, i.e., maximum attenuation and minimum RF output power. This allows the TGC control to bring the RF level up from start. In the case of PRESET POWER, the counters are preset to a level that provides immediate RF power, which is then adjusted with normal TGC action.

(4) "Dead Zone" acquisition selects SLOW clock. When the RF sample falls within the TGC detector "dead zone" for the time equivalent to the time constant of R127/C22, the U7A fast clock command is reset (deselected). The U7A RESET command places the U7A Q-NOT output at logic high. This releases the U7A fast clock command and the clock returns to normal operation. A (-) output of AR11A and AR11B indicates that the RF output power is now in the "dead zone" (figure 5-8). The AR11 output is processed, inverted by U10A, and NANDed at U10B with the IF sample detector. If the IF level is within 20 dB of full power (logic 1), and the "dead zone" is achieved (logic 1), the output of U10B is logic low, and inverted by U10C to logic high. This output is then NANDed by U10D with the counter CARRY OUT, which is logic 1 except at the end stops of the counter. Assuming the end stops have not been reached, the output of U10D is logic low and is applied to the R127/C22 time constant, where C22 now discharges through R127. At the end of the time constant, the input to inverter U8C is logic low, placing a RESET command on U7A-4; i.e., the U7A fast clock command is no longer selected.

(5) PPC detection commands FAST clock. The PPC output, via CR18, is routed to voltage comparator AR8B. The threshold of AR8B is set by R132/R133. When the PPC voltage exceeds the threshold level, the output of AR8B is +15 Vdc, which is routed via R128 to R129 and Q7. This PPC condition illuminates LED DS1 and turns on transistor Q7. With transistor Q7 turned on, diode cathodes CR63 and CR64 are brought to ground to select count down (CR64) and fast clock (CR63). Therefore, when PPC is detected, an immediate correction is made giving the TGC circuit a head start towards reducing the RF output level

o. TGC Bit Detector. The previous discussion for generating the RESET command for U7A applies directly to the generation of the TGC BIT output. The BIT output, from NAND U10D, is a logic low for a successful BIT test. Therefore, BIT verifies that a "dead zone" is achieved, a nominal IF sample is present, and the counter end stops are not reached.

p. TGC Counters. Counters U5 and U6 form the digital element of the digital-to-analog conversion used to generate the TGC voltage. The digital outputs of U5 and U6 (8 bits, 256 states) are converted to analog by U11. Counters at low count result in maximum PIN diode attenuation and low RF

levels. Counters at high count result in minimum PIN diode attenuation and high RF levels. For a typical counter sequence, a RESET POWER command places the RF output power level at a minimum, since the PIN diodes will be at maximum attenuation. When the transmitter is keyed, the TGC detector calls for more RF output power with a clock enable and a count up command. Additional logic circuits command the fast clock speed. When the RF output power sample falls within the TGC detector "dead zone", the counter clock is disabled and the counter stops. During this entire sequence, the counter output is converted to an analog voltage which is used to bias the PIN diode attenuators. Once the "dead zone" is reached, the output analog voltage is steady, and the fine tuning of the counter is accomplished by slow clock. The logic inputs to the clock are as follows:

(1) The COUNT UP/COUNT DOWN control at U5-10, U6-10, comes from the AR11A output. The AR11A output (after diode and voltage divider processing) is (+) (count up) when the RF sample is less than the IF sample, indicating an increase is needed in the RF output power level. When the AR11A output is (-), the RF sample is greater than the IF sample, and a count down (0 Vdc) signal is applied to the counters, indicating a decrease is needed in the RF output power level (figure 5-8).

(2) The logic high U1 command RESET POWER resets the counters to zero (Q outputs 00000000). The logic high U1 command PRESET POWER inserts the counter "P" inputs into the counter registers (Q outputs 10100000) and thereby sets the RF output power at a level somewhat higher than the normal. This allows a rapid rise in RF output power, which is then reduced to a normal operating level through the PPC and TGC control action.

q. Digital-to-Analog Conversion.

(1) The counter has an 8-bit digital output. This allows 256 different counter states, all of which can be converted into an analog current by U11. Conversion from current to voltage is accomplished by AR13A. The resulting TGC voltage ranges from 0 to +10 Vdc, where a counter reset equals 0 Vdc, and a count of 255 equals +10 Vdc. The 0 to +10 Vdc TGC voltage is converted to -6 Vdc to +6 Vdc by inverter AR13B and driver transistors Q10/Q11. The +6 Vdc level represents maximum PIN diode attenuation (minimum RF output level), and -6 Vdc represents minimum PIN diode attenuation (maximum RF output level).

(2) The AR13B (+) reference input is also used to add a PPC power correction to the output TGC control voltage by changing the reference level. This PPC power correction has the immediate effect of lowering the RF output power level during an excessive peak output. The power level is held until the TGC voltage can make the long-term correction through clock-down action. Transistor Q9 acts as the PPC emitter follower, fed via R233 and loop filter R139/C26/C74/R234.

(3) An additional input at the AR13B (+) threshold is a "half-step" voltage from U8D. Since the 8-bit counter can have 256 different outputs, the analog output can have 256 different voltage levels. It is possible to add or subtract a voltage equal to 1/2 of one of the 256 different voltage levels, thereby giving the effect of having a 9-bit counter output and 512 different voltage levels.

(4) The inputs to U8D include the TGC clock and the Q-NOT output of "D" flip flop U7B. The U7B "D" input is the up/down clock control line. When the up count is applied to the "D" input (logic high), the Q-NOT output is logic low, enabling the "add" 1/2 step feature. When the down count is applied to the "D" input (logic low), the Q-NOT output is logic high, enabling the "subtract" 1/2 feature. A logic low (from U7B) into U8D causes it to act as a non-inverting buffer for the clock input. Conversely, a logic high causes U8D to act as an inverting buffer to the clock input. Therefore, every half cycle of the clock will either be added or subtracted as a half step to AR13B.

(5) The output inverter and driver AR13B/Q10/Q11 also has a TGC clamp circuit on the input to AR13B. This circuit (Q27/Q28 and their associated components), when activated by a logic 1 from U1 pin 11, will jam the TGC output voltage to approximately midrange. This clamp circuit is normally used only during the BIT tests on the First Converter and Exciter Boards to reduce the possibility of a TGC failure influencing the other BIT tests.

r. MCB Interface. The byte used to control the TGC functions is applied to serial-to-parallel converter U1. The Module Control Bus (MCB) interface for the TGC circuit is located on Exciter PWB A1A1. The MCB loads U1 registers through a serial data stream and MCB clock. After loading, a strobe latches the serial data into the U1 parallel storage registers. The

resulting parallel outputs are the control signals discussed in previous paragraphs.

s. Power-up Detector. When +5 Vdc supply power is first applied to the AGC/TGC PWB, the counter RESET line is held at logic high by the output of U12C. The logic high continues until capacitor C14 is charged through resistor R86. After C14 is charged, the output of U12C is logic low, the RESET condition is removed, and normal circuit operation is enabled. This start sequence assures that the TGC counters do not assume a random number during power-up, which would allow the TGC voltage to enable an uncontrolled RF output level. C14 is also connected via CR37 to the Vcc sense/overvoltage protection circuit. Should Vcc exceed the overvoltage threshold, Q29 will turn on and discharge C14 through CR37.

5-40. RECEIVER PWB ASSEMBLY, A1A7, 10085-5200. This manual portion describes the Receiver PWB as an individual assembly. Section I of this chapter describes the function of the Receiver PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram	Figure 5-9
b. Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
f. Overall Interconnection	Figures FO-11,FO-12
g. Transceiver Assembly Schematic Diagrams	Depot Manual

5-41. OVERALL RECEIVER PWB FUNCTION. The purpose of the Receiver PWB (figure 5-9) is to provide detection of the received RF signal yielding audio outputs for the front panel speaker and headphone and for external audio connections. The functions of the Receiver PWB are as follows:

a. Conversion of 40.455 MHz IF to 455 KHz IF.

b. Conversion of 455 KHz IF to SSB and AM audio signals.

c. Generation of the AGC DETECTOR output.

d. Control IF signal levels with 1st IF AGC and 2nd IF AGC.

e. Generation of LINE, AUDIO 2, AUX, HEADPHONE, and SPEAKER audio outputs.

f. Generation of SQUELCH function.

5-42. OVERALL RECEIVER PWB OPERATION.

a. MCB Interface. The interface between the A1A12 Control PWB and the A1A7 Receiver PWB is through MCB, using MCB address "1". The MCB write functions yield 16 bits of data that are latched into output parallel registers and used as control signals throughout the Receiver PWB. The MCB uses an 8-bit interface for BIT read back from the Receiver PWB, and other PWB's that have their BIT outputs routed to the Receiver PWB for readback.

b. IF Conversion. The 40.455 MHz 1st IF is converted to a 455 KHz 2nd IF on the Receiver PWB. The input LO is a reference frequency of 40.00 MHz. The 455 KHz 2nd IF then exits the board for filtering on the IF Filter PWB A1A2. After filtering, the 455 KHz signal is returned to the Receiver PWB and applied to a product detector and envelope detector.

c. AGC Control. The AGC is applied to both the 1st IF signal (40.455 MHz), using a -6 Vdc to +6 Vdc control voltage, and the 2nd IF signal (455 KHz) using a 0 to -10 Vdc signal. Both AGC attenuators consist of PIN diode networks. A complete description of the AGC control circuits is given in the discussion on the A1A6 AGC/TGC PWB.

d. BIT Detector. The BIT detector for the Receiver PWB is generated by sampling the 455 KHz IF output with a peak detector and switch. If the 455 KHz is present, the BIT switch will close placing a logic low at the MCB readback port.

e. Audio Detectors. A product detector is used for detection of single sideband signals. The input BFO is 455 KHz, plus or minus any entered BFO offset. The BFO signal is under MCB control with a BFO DISABLE signal. The envelope detector output is selected only in the AME mode of operation;

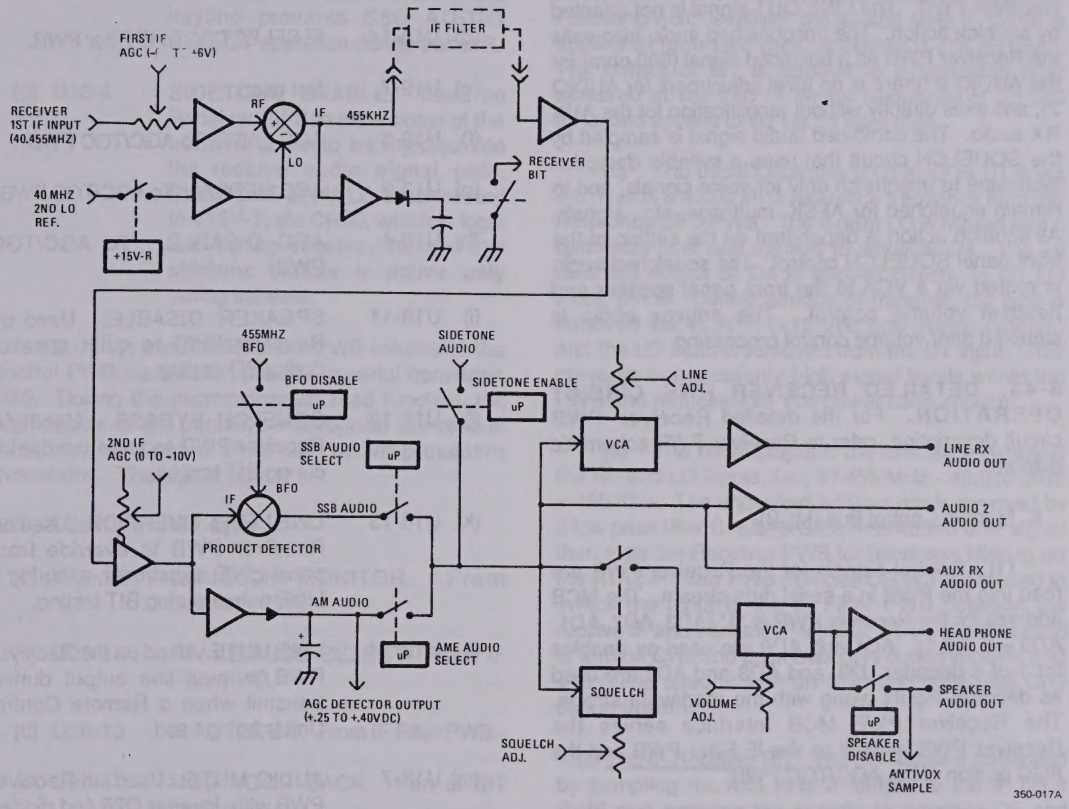


Figure 5-9. Simplified Receiver PWB Diagram

however, the circuit is always active since the AGC DETECTOR output is derived from the AME detector.

f. Audio Processing. The product and envelope detector outputs are selected by MCB control. The combined audio signal, including a TX audio sample used for the sidetone feature, is routed to three locations. The LINE OUT signal is passed through a Voltage Controlled Amplifier (VCA) and exits the Receiver PWB. The LINE OUT signal is not affected by squelch action. The unsquelched audio also exits the Receiver PWB as a balanced signal (600 ohm) for the AUDIO 2 (there is no level adjustment for AUDIO 2), and exits directly without amplification for the AUX RX audio. The combined audio signal is sampled by the SQUELCH circuit that uses a syllabic detection technique to unsquelch only for voice signals, and to remain squelched for AFSK, multitone, etc., signals. All squelch action is dependent on the setting of the front panel SQUELCH control. The squelched audio is routed via a VCA to the front panel speaker and headset volume control. The antivox audio is sampled after volume control processing.

5-43. DETAILED RECEIVER PWB CIRCUIT OPERATION. For the detailed Receiver PWB circuit description, refer to Receiver PWB schematic diagram.

a. Module Control Bus (MCB).

(1) Control signals for the Receiver PWB are read into the PWB in a serial data stream. The MCB address for the Receiver PWB is "1" (AD3, AD2, AD1, AD0 = 0,0,0,1). AD1 and AD0 are used as enables for 1-of-8 decoder U23, and AD3 and AD2 are used as decoder inputs along with the read/write strobe. The Receiver PWB MCB interface serves the Receiver PWB as well as the IF Filter PWB and the AGC portion of the AGC/TGC PWB.

(2) When MCB data is intended for the Receiver PWB MCB interface, decoding generates the desired enables for the bus registers. The clock signal then clocks in 16 serial bits of data into the U18/U19 shift register ports. The first data bit is clocked to the last U19 bus register port and is used as part of the Receiver MCB loop back BIT test sequence (Q8 output of register U19). After all the data is clocked in, the "write" strobe is decoded and the data in the bus registers is latched into the bus storage registers and appears at the bus register output pins as steady control voltages. The MCB data outputs for the Receiver PWB are as listed below (in order of MCB serial entry).

(a) U19-11 MCB LOOP BACK. Part of BIT testing.

(b) U19-12 IF ENABLE. To IF Filter PWB.

(c) U19-13 IF SELECT 1. To IF Filter PWB.

(d) U19-14 IF SELECT 0. To IF Filter PWB.

(e) U19-7 Not used.

(f) U19-6 AGC FAST. To AGC/TGC PWB.

(g) U19-5 AGC MEDIUM. To AGC/TGC PWB.

(h) U19-4 AGC DISABLE. To AGC/TGC PWB.

(i) U18-11 SPEAKER DISABLE. Used on Receiver PWB to quiet speaker during BIT testing.

(j) U18-12 SQUELCH BYPASS. Used on Receiver PWB to force unsquelch during BIT testing.

(k) U18-13 LINE LEVEL OVERRIDE. Used on Receiver PWB to override front panel LINE adjustment, assuring a LINE output during BIT testing.

(l) U18-14 LINE MUTE. Used on the Receiver PWB to mute line output during transmit when a Remote Control Unit is being used.

(m) U18-7 AUDIO MUTE. Used on Receiver PWB with inverter Q26 and diodes CR28/CR29 to mute both SSB, and AM audio outputs during BIT testing, frequency changes,etc.

(n) U18-6 AM AUDIO SELECT. Used on Receiver PWB to select AM envelope detector audio output. A RC delay is inserted to select audio only after circuit stabilization. Connection via diode CR 30 to the keyline prevents AM AUDIO SELECT operation during transmit.

(o) U18-5 SSB AUDIO SELECT. Used on Receiver PWB to select SSB product detector audio output. A RC delay is inserted to select audio only after circuit stabilizatioin. Logic is inverted to form BFO DISABLE so that the BFO function is not active in the AME mode. Connection via diode CR31 to the keyline prevents SSB AUDIO SELECT operation during transmit.

(p) U18-4 SIDETONE ENABLE. Used on Receiver PWB to allow some of the transmit audio to be injected into the receive audio signal path. SIDETONE ENABLE is connected to +15V-T, via CR36, which is logic low during receive; hence, the sidetone feature is active only during transmit.

(3) Data from the Receiver PWB returns to the control PWB via an 8-bit parallel-to-serial converter, U20. During the microprocessor read function, the eight inputs to the parallel/serial register are read in serial to the Control PWB for micvroprocessor processing. The eight inputs are:

(a) U20-1 Not used

(b) U20-15 SQUELCH MONITOR. From Receiver PWB.

(c) U20-14 CW LSB/USB SELECT. From IF Filter PWB.

(d) U20-13 IF FILTER BIT. From IF Filter PWB.

(e) U20-4 MCB LOOP BACK. Part of BIT testing.

(f) U20-5 RECEIVER 2ND IF BIT. From Receiver PWB.

(g) U20-6 RX 1ST IF BIT. From 1st Converter PWB.

(h) U20-7 TX RF BIT. From 1st Converter PWB.

b. 2nd Receiver Mixer.

(1) Conversion of the 1st IF 40.455 MHz to a 455 KHz 2nd IF is accomplished by mixer U1. The 40.455 MHz 1st IF input is routed from the 1st Converter PWB via J1. The 40.455 MHz signal is first applied to a 40 dB AGC attenuator, CR1/CR2. The AGC control voltage ranges from -6 Vdc (minimum attenuation) to +6 Vdc (maximum attenuation). The generation and injection of the AGC control voltage is described in A1A6 AGC/TGC PWB discussion. Following AGC levelling, the 40.455 MHz IF signal is applied to grounded gate amplifier Q1 (12 dB gain). The output of Q1 is applied to a bandstop filter centered at the 2nd IF image frequency of 39.545 MHz, and applied to U1 via an input filter.

(2) The Local Oscillator (LO) input to U1 is via J4. This is a 40.00 MHz reference frequency from the Reference/BFO PWB. The 0 dBm LO is filtered with a bandpass filter and applied to amplifier Q4. The +6 dBm LO output of Q4 is applied directly to U1 LO input, pin 8. During periods of transmit, Q4 bias is removed via +15V-R (+15 Vdc only during receive) and the LO input is removed from the U1 input. This prevents unnecessarily high signal levels within the PWB and reduces +15 Vdc power consumption.

(3) The U1 IF output is the difference between the RF and LO inputs, i.e., 40.455 MHz - 40.000 MHz = 455 KHz. The undesired additive mix is removed by a low pass filter C18/L13/C20. The 455 KHz IF signal then exits the Receiver PWB for bandpass filtering on the A1A2 IF Filter PWB. Diodes CR3/CR4 are used to switch the input to the IF Filter PWB between the receive IF and transmit IF signals. The +15V-R is used to turn on CR3 and back bias CR4 during receive, and +15V-T is used to turn on CR4 and back bias CR3 during transmit.

(c) 2nd IF Receiver BIT. The BIT signal is generated by sampling the 455 KHz IF output to the IF Filter PWB and applying the sample to amplifier Q5 and detector CR5/CR6. During BIT sequencing, the detected voltage turns on transistor Q6, and the desired logic low is routed to the MCB readback port, U20-5.

(d) Audio detection. Audio detection of the 455 KHz IF is accomplished by either a product detector (for SSB signals) or an envelope detector (for AM signals).

(1) After filtering on the IF Filter PWB, the 455 KHz signal reenters the Receiver PWB at J5. Switching diodes CR7 and CR8 select the TX or RX IF

signal path in a manner similar to the diode action of CR3/CR4. In receive, the input 455 KHz IF is applied to grounded gate amplifier Q8. The output of Q8 is applied to three stages of AGC controlled amplification. The Q9/Q10/Q11 amplifiers are gain adjusted (60 dB dynamic range) by PIN diodes CR9/CR10/CR11. The AGC control voltage is 0 V (minimum attenuation) to -10 Vdc (maximum attenuation). The maximum attenuation is set by AGC ADJUST R197. Refer to the AGC/TGC PWB circuit description for a discussion of this AGC control voltage. The gain of the amplifier chain is set by R42 GAIN ADJUST.

(2) The output of amplifier Q11 is bandpass filtered by L24/L25 and associated components, to remove any wideband noise, and applied to buffer amplifier Q12, for SSB audio detection, and to Q14 for envelope detection. Q11 output can be measured at TP1 with a high impedance probe. The nominal voltage at TP1 is 35 millivolts, peak-to-peak, with an input level at J5 of -80 dBm. Buffer amplifier Q12 has a gain of one; however, it exhibits high reverse isolation and thereby prevents U2 mixer frequency components from feeding back into the Q9-Q11 amplifiers. The output of Q12, via 50 ohm impedance matching components L32/C63, is applied to mixer (product detector) U2.

(3) The BFO input to product detector U2 is 455 KHz at center frequency. In the CW mode, the BFO center frequency is offset to 454 KHz or 456 KHz, depending on the sideband selection switch position on the IF Filter PWB. The operator may also add BFO offset through the use of the front panel BFO feature (plus or minus 1 KHz). After amplification by Q13, the BFO is applied to mixer U2. The base of Q13 can be brought to ground by the uP control signal BFO DISABLE. The BFO is disabled in the AME mode by BFO DISABLE.

(4) The U2 product detector functions as a mixer with the difference between the 455 KHz IF and 455 KHz BFO as an output, i.e., the sideband audio. The audio is filtered by a low pass filter R73/C69 to remove the additive output of U2, and by high pass filter C70/R74. The resulting audio is then amplified by AR1 forming the final Single Sideband Audio output of 75 millivolts RMS as measured at TP2.

(5) The 455 KHz IF to the envelope detector is amplified by Q14/Q15 and applied to envelope detector Q16. The base-emitter junction of Q16 forms the detection diode. This method is used to linearize the detector response, since the detector (Q16) is always biased into conduction. The resulting envelope then exits the Receiver PWB as the AGC DETECTOR output, and is low pass filtered by R86/C78 for the AM audio output. The R86/C78 filter removes any 455 KHz components remaining on the detected audio. Note that the envelope detector circuit is always active, no matter what the mode of operation. This is done to assure an AGC DETECTOR output. Since the AGC DETECTOR output is derived from the IF frequency (455 KHz), it is called IF derived AGC.

e. Audio Output Processing. A number of microprocessor control signals (from U18) are now used to guide the audio through various audio output circuits. In addition, the SQUELCH feature is generated and used as a control signal. A review of figure 5-9 will illustrate what audio signals are under squelch control, front panel control, etc.

(1) The primary audio inputs, SSB and AM, are applied to switch U4. The uP control signal AM AUDIO SELECT (logic high) enables the AM audio path from U4-1 to U4-15. The uP control signal SSB AUDIO SELECT (logic high) enables the SSB audio path from U4-3 to U4-4. The two audio output lines are connected, plus an additional audio input is injected from the sidetone feature. When sidetone is desired (only during transmit), a portion of the TX audio is fed into the RX audio path to produce an audio signal for the operator. In the CW mode, the audio signal is a 1 KHz tone. The sidetone audio input is first amplified by AR2 where SIDETONE LEVEL adjust R93 sets the AR2 gain, and is then applied to switch U4. SIDETONE ENABLE (logic high) enables the audio path from U4-13 to U4- 14 and the sidetone audio is combined with the selected AM and SSB audio path. The primary audio node at U4-4/15 now branches out to a number of audio processing destinations.

(2) The primary audio node is tapped by C85 and routed to Voltage Controlled Amplifier (VCA) AR3. The gain of AR3 is determined by the positioning of the front panel LINE adjustment. After amplification by AR3, the output audio is further amplified by AR9A and exits the Receiver PWB at RX LINE OUT at a maximum level of +16 dBm. During BIT testing, the LINE OUT audio path is tested. Since it is possible that the operator may turn the front panel LINE adjustment to minimum and thereby induce a BIT failure, a control signal LINE LEVEL OVERRIDE is used to fix the gain of AR3 in BIT. The level of LINE

OUT is tapped by voltage follower AR9B and, after additional processing on another assembly, is used for the front panel LINE meter display.

(3) The primary audio node is also tapped by resistor R188. From R188, the audio is routed directly to AR10A for amplification and to output transformer T2. Transformer T2 serves the function of converting the unbalanced audio into a 600 ohm balanced audio output. This is designated the AUDIO 2 output and is fixed at a level of +12 dBm. Further processing of the AUDIO 2 RX AUDIO is completed at the A1A1 Exciter PWB. From R188, the audio is also routed to voltage follower AR10B. The output of AR10B exits the Receiver PWB as the AUXILIARY RX AUDIO port.

(4) The primary audio node is also tapped by switch U5. The operation of switch U5 is determined by the squelch circuit. When the squelch feature is used, the audio connection between U5-12 and U5-14 is made only with the receiver unsquelched. Assuming this condition, the U5 switched audio is routed to VCA AR12. The gain of AR12 is determined by the front panel setting of the VOLUME control. The +1.8 Vdc reference of AR12 prevents the control voltage from dropping below +1.8 Vdc, where the VCA would exhibit a reverse gain characteristic. The output of AR12 is amplified by AR8 for the HEADPHONE RX AUDIO output, and applied to another portion of switch U5. The uP output SPEAKER DISABLE is inverted by Q27 and used to open the U5-3 to U5-4 connection, i.e., disable the front panel speaker. The SPEAKER DISABLE command is generated during BIT testing to mute the front panel speaker. The connection of diode CR34, at the output of Q27, to J11-5 can also cause the front panel speaker to be disabled if a handset is connected at the transceiver front panel. A front panel SPKR switch can also be used to turn off the front panel speaker. A sample of the front panel speaker audio is used for the ANTIVOX circuit, and exits the Receiver PWB at P1-10. Front panel speaker amplifier AR11 has a frequency equalizing feedback network. The 8 watt AR11 output can drive a speaker load as low as 1.6 ohms.

(5) The primary audio node is also tapped through C107 as the audio sample input for the squelch circuit. Operation of the squelch circuit, is explained in the description that follows.

f. Squelch circuit. Amplifiers AR4, AR5 and AR6 form an adjustable syllabic squelch circuit. The front panel SQUELCH control is used to set the threshold level of the circuit, or the OFF (detent) position can be selected if no squelch action is needed. In addition, a uP control signal SQUELCH BYPASS can override a squelched condition and place the equipment into an unsquelched condition; however, there is no control signal to force the equipment into a squelched condition. A syllabic squelch circuit operates by processing the syllabic content in the audio signal. For voice communications, detected syllabic content in the 5-18 Hz range indicates the presence of a normal speech pattern. Therefore, the receiver will unsquelch only if speech audio is detected, and will remain squelched if sustained single tone, multitone, or similar audio signals are detected. When the squelch feature is selected, the circuit operates by exceeding the level established by the setting of the front panel SQUELCH control.

(1) The audio sample is first applied to an audio compressor circuit consisting of AR4A, Q19 and Q20. The output of the audio compressor is then peak detected by the combination of AR4/CR14/CR15, which operates as a full wave rectifier. The rectifier strips off the envelope and peak detects the audio sample.

(2) The peak detected audio signal is applied to active bandpass filter AR5A and associated components. The bandpass filter has an output only if the peak detected signal has content within a 5 to 18 Hz frequency range. For example, if the peak detected signal is a steady dc level, then there is no output of the bandpass filter at AR5A, and the receiver will not unsquelch.

(3) The output of the active bandpass filter is applied to another full wave rectifier AR5B/CR16/CR17, where the peak amplitude is again detected. If sufficient dc is developed, the output of AR6A exceeds the threshold input at AR6B (+), and the receiver becomes unsquelched.

(4) The output squelch dc from amplifier AR6A is compared with a voltage reference in voltage comparator AR6B. The threshold reference input for AR6B (+) comes from the front panel SQUELCH adjustment, via dc processing by AR7A. When the dc from the squelch circuit exceeds the AR6B (+) voltage reference, the output of AR6B switches to -15 Vdc to unsquelch the receiver. During squelch, the output of AR6B is +15 Vdc.

(5) The AR6B output is applied to the fast attack/slow decay network at the input to AR7B. This

network allows the receiver to rapidly unsquelch, but to squelch again only after a short delay. The output of AR7B is -15 Vdc for unsquelch and +15 Vdc for squelch. Squelch switch U5 opens when +5 Vdc is applied to U5-11, i.e., the squelch condition. To unsquelch U5, the control signal must be pulled to ground potential. When the output of AR7B is -15 Vdc (unsquelch), U5-11 is pulled to ground via CR21 (CR33 is used to clamp off the AR7B output). When a SQUELCH BYPASS is applied to Q18 (logic high), the transistor is turned on and the U5-11 control input is grounded, i.e., the circuit is unsquelched. The last condition that can unsquelch the circuit is the CONDITIONED KEYLINE input. When the transmitter is keyed, the audio circuit is automatically unsquelched. This is necessary because the sidetone goes through the U5 squelch gate. The SQUELCH MONITOR output is for future use, should an external indication be needed of the receiver squelch condition. This line cannot be used for external squelch control.

5-44. CRYSTAL OSCILLATOR ASSEMBLY A1A8, 10085-0610. This manual portion describes the Crystal Oscillator Assembly as an individual unit. Section I of this chapter describes the function of the Crystal Oscillator Assembly in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Crystal Oscillator Connection Diagram	Figure 5-10
b. 100 Watt Transceiver Simplified Block Diag.	Figure FO-1
c. Overall Interconnection	Figures FO-11,FO-12
d. Transceiver Assembly Schematic Diagrams	Depot Manual

5-45. OVERALL CRYSTAL OSCILLATOR ASSEMBLY FUNCTION. The purpose of the Crystal Oscillator Assembly is to provide a highly stable 10.000,000 MHz reference frequency from which a variety of transceiver injection frequencies are derived. Injection frequency generation is discussed for Reference/BFO PWB A1A9 and Synthesizer PWB A1A10. The crystal oscillator is enclosed in an oven for temperature stabilization. During power up, a warm-up period of up to 20 minutes is required to obtain frequency stability. This warm-up time is dependent on ambient temperature.

5-46. DETAILED CRYSTAL OSCILLATOR CIRCUIT DESCRIPTION. The Crystal Oscillator Assembly is a sealed unit. If it fails, it is replaced as a unit. The connections to the unit are shown in figure 5-10.

5-47. CRYSTAL OSCILLATOR SUMMARY OF SPECIFICATIONS. Below is a summary of Crystal Oscillator Assembly specifications:

a. Output Frequency - 10.000,000 MHz

b. Frequency Stability

(1) Temperature - 3.3 parts in 10,000,000 over the entire operating range of -30 to +75 degrees centigrade.

(2) Long Term - 1 part in 100,000,000 per day, 5 parts in 100,000,000 during the first 30 days after calibration, and no more than 4 parts in 100,000,000 per each 30-day period thereafter.

c. Calibration - An externally accessible frequency adjustment, located on the top of the unit, permits periodic calibration and alignment within 1 part in 100,000,000 for a period of at least 12 years.

d. Output Signal Level - Sine wave output of 0.6 to 1.0 V pk-pk measured across a 1 kilohm resistance.

e. DC Supply Voltages -

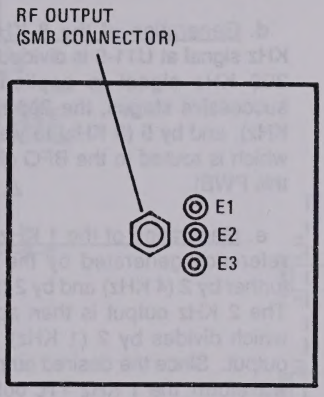
(1) Oven voltage: +10.0 to +16.0 Vdc

(2) Oscillator and oven control voltage: +15.0 +/-0.5 Vdc

f. Input Current - 800 milliamperes, absolute maximum at turn-on at any temperature.

g. Warm Up - Frequency error from exactly 10.000,000 MHz is less than 6.6 parts in 10,000,000, in 20 minutes or less after turn-on from any temperature in the operating range of -30 to +75 degrees centigrade.

5-48. REFERENCE/BFO PWB ASSEMBLY, A1A9, 10085-5500. This manual portion describes the Reference/BFO PWB as an individual assembly. Section I of this chapter describes the function of the Reference/BFO PWB in relation to overall transceiver operation. The following



E1	+15 VDC (OVEN CONTROL AND OSCILLATOR VOLTAGE)
E2	GND
E3	+13.6 VDC (OVEN VOLTAGE)

350-049A

Figure 5-10. Crystal Oscillator Connection Diagram (Bottom View)

references apply for the detailed discussion that follows:

a. Simplified Reference Diagram	Figure 5-11
b. Simplified BFO Diagram	Figure 5-12
c. Reference/BFO Schematic Diagram	Depot Manual
d. Parts List	Depot Manual
e. Component Layout	Depot Manual
f. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
g. Overall Interconnection	Figures FO-11 and FO-12
h. Transceiver Assembly Schematic Diagrams	Depot Manual

5-49. OVERALL REFERENCE FUNCTION. The purpose of the Reference portion of the assembly is to generate four fixed reference frequencies required for the operation of the other transceiver assemblies. The reference frequencies are all generated from an input 10 MHz crystal oscillator frequency standard (assembly A1A8). The four reference frequencies are:

a. 40 MHz 2nd LO to the Exciter and Receiver PWB's.

b. 200 KHz reference to the Synthesizer PWB.

c. 8 KHz reference to the BFO portion of the Reference/BFO PWB.

d. 1 KHz reference to the Exciter PWB.

5-50. DETAILED REFERENCE CIRCUIT OPERATION. For the detailed Reference circuit description, refer to the Reference/BFO PWB schematic diagram.

a. 10.000.000 MHz frequency standard input processing. The input 10.000,000 MHz from frequency standard A1A8 is applied to the gate of source follower Q21. The output of Q21 drives a two-stage amplifier consisting of Q22A and Q22B, where the 10 MHz sine wave is converted to a TTL output. The TTL output is then buffered by U14A/D and applied to the reference generating circuits.

b. Generation of the 40 MHz 2nd LO. The 10 MHz standard frequency is applied to buffer transistor Q1, which is configured as an emitter follower with an R1/C1 integrator network at the base input. This converts the TTL input into a triangle waveform output at the Q1 emitter that is rich in even harmonics. Transistor Q2 is configured as a class C amplifier, with a double tuned circuit at the output, tuned for the 4th harmonic of the 10 MHz, i.e., the desired 40 MHz output. The 40 MHz then exits the PWB at connectors J3 and J4.

c. Generation of the 200 KHz reference. The 10 MHz TTL standard frequency is used as an input to divider U11. In successive stages, the 10 MHz is divided by 5 (2 MHz), by 5 (400 KHz) and by 2 (200 KHz) to yield the 200 KHz reference which exits the PWB at pendant cable P2.

d. Generation of the 8 KHz reference. The 400 KHz signal at U11-9 is divided by 2, and the resulting 200 KHz signal is applied to divider U12. In successive stages, the 200 KHz is divided by 5 (40 KHz), and by 5 (8 KHz) to yield the 8 KHz reference which is routed to the BFO circuitry (also located on this PWB).

e. Generation of the 1 KHz reference. The 8 KHz reference generated by the divider U12 is divided further by 2 (4 KHz) and by 2 (2 KHz), also within U12. The 2 KHz output is then applied to flip flop U13B which divides by 2 (1 KHz), yielding a 1 KHz TTL output. Since the desired output is a 1 KHz sinewave waveform, the 1 KHz TTL output is filtered by active filter AR1A, and after BIT sampling, exits the PWB at connector J5.

5-51 . OVERALL BFO FUNCTION. The BFO circuit is used during transmit as a 455 KHz carrier generator, and during receive as a 455 KHz BFO generator. The center frequency of 455 KHz is adjusted depending of the mode of operation. When transmitting in single sideband modes (USB, LSB), the carrier frequency is 455 kHz. When transmitting in CW mode, the carrier frequency is 456 KHz for USB derived CW, and 454 KHz for LSB derived CW. When transmitting in the AFSK, the carrier frequency is also shifted as described in section A1A18 AFSK Assembly. During receive, the BFO center frequency is 455 KHz for the SSB modes, 454 KHz or 456 KHz for the CW mode, and other center frequencies for the AFSK mode as described in section A1A18. In all receive modes,

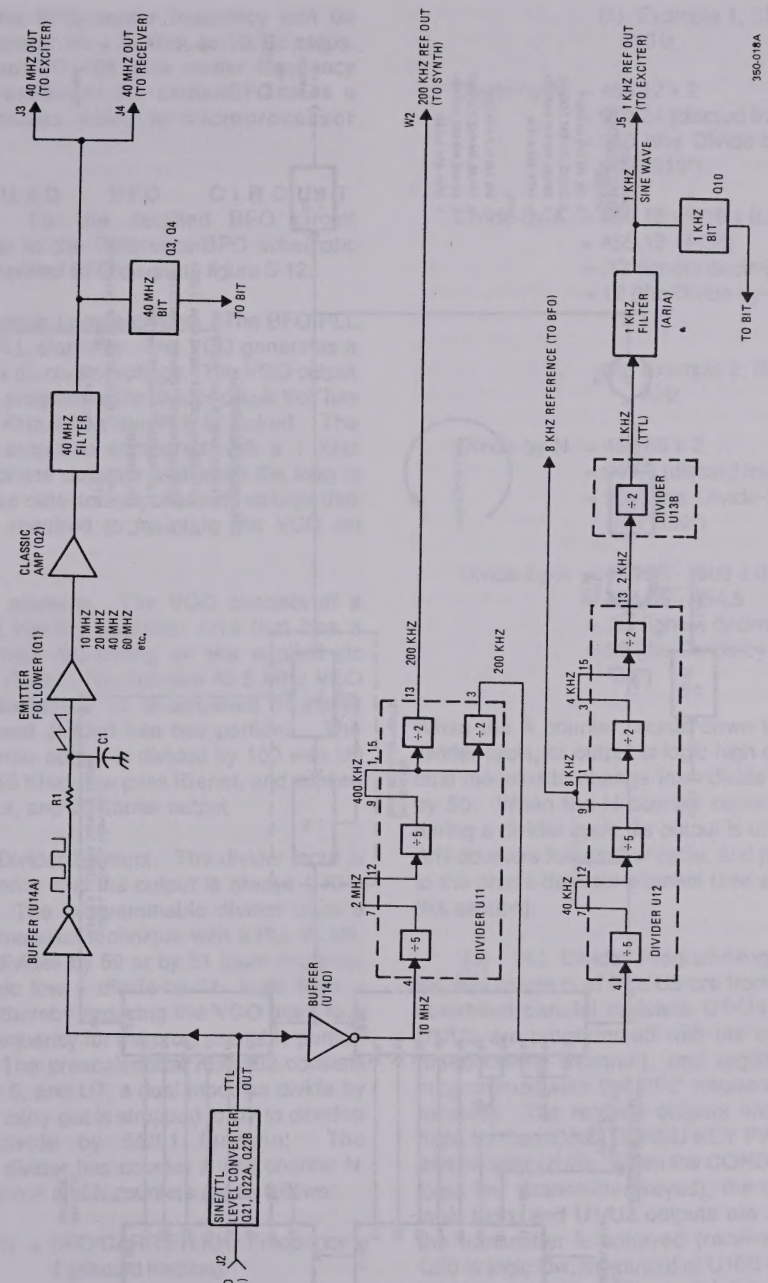


Figure 5-11. Simplified Reference Output Operation

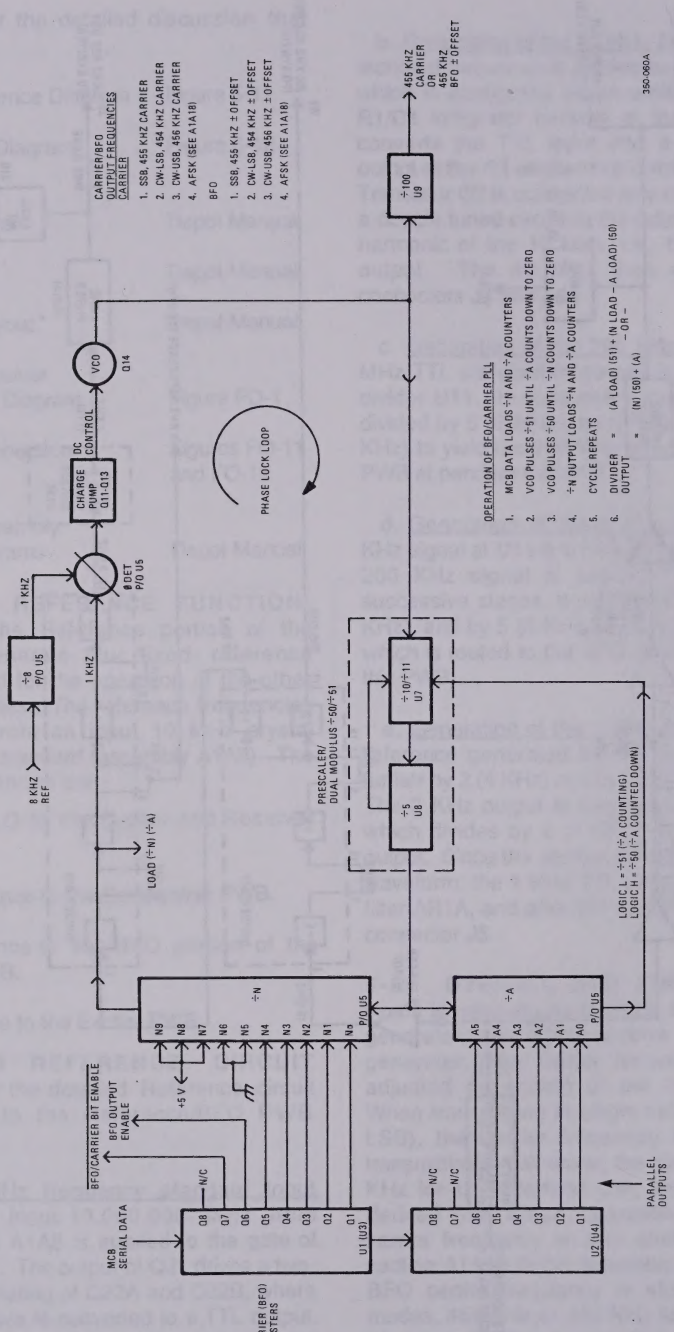

CARRIER/BFO OUTPUT FREQUENCIES
CARRIER
1. SSB, 455 KHZ CARRIER
2. CW-LSB, 454 KHZ CARRIER
3. CW-USB, 456 KHZ CARRIER
4. AFSK (SEE A1A1B)
BFO
1. SSB, 455 KHZ ± OFFSET
2. CW-LSB, 454 KHZ ± OFFSET
3. CW-USB, 456 KHZ ± OFFSET
4. AFSK (SEE A1A1B)
455 KHZ CARRIER OR 455 KHZ BFO ± OFFSET
÷100 U9
VCO Q14
DC CONTROL
CHARGE PUMP Q11-Q13
Φ DET P/O U5
PHASE LOCK LOOP
1 KHZ
÷8 P/O U5
8 KHZ REF
LOAD (÷N) (÷A)
PRESCALER/ DUAL MODULUS ÷50/÷51
÷10/÷11 U7
÷5 U8
OPERATION OF BFO/CARRIER PLL
1. MCB DATA LOADS ÷N AND ÷A COUNTERS
2. VCO PULSES ÷51 UNTIL ÷A COUNTS DOWN TO ZERO
3. VCO PULSES ÷50 UNTIL ÷N COUNTS DOWN TO ZERO
4. ÷N OUTPUT LOADS ÷N AND ÷A COUNTERS
5. CYCLE REPEATS
6. DIVIDER OUTPUT = (A LOAD) (51) + (N LOAD – A LOAD) (50) – OR – = (N) (50) + (A)
LOGIC L = ÷51 (÷A COUNTING)
LOGIC H = ÷50 (÷A COUNTED DOWN)
÷N
÷A
P/O U5
+5 V
BFO/CARRIER BIT ENABLE
BFO OUTPUT ENABLE
MCB SERIAL DATA
N/C
U1 (U3)
U2 (U4)
CARRIER (BFO) REGISTERS
PARALLEL OUTPUTS
350-0604A

Figure 5-12. Simplified BFO/Carrier Operation

except AME, the BFO center frequency can be adjusted from center by + 1 KHz, in 10 Hz steps. Since the carrier/BFO 455 KHz center frequency varies, the generation of the carrier/BFO uses a phaselock technique which is microprocessor controlled.

5-52. DETAILED BFO CIRCUIT OPERATION. For the detailed BFO circuit description, refer to the Reference/BFO schematic diagram, and simplified BFO diagram, figure 5-12.

a. BFO Phaselock Loop elements. The BFO PLL uses standard PLL elements. The VCO generates a frequency from a dc control voltage. The VCO output is sampled by a programmable divider circuit that has an output of 1 KHz when the PLL is locked. The divider 1 KHz output is compared with a 1 KHz reference in a phase detector and when the loop is locked, the phase detector output is a dc voltage that is exactly that required to maintain the VCO on frequency.

(1) VCO element. The VCO consists of a varactor tuned Hartley oscillator Q14 that has a variable frequency depending on the applied dc voltage, via L4 (TP2). The nominal 45.5 MHz VCO output from transformer T1 is amplified by buffer amplifier Q15 and divided into two portions. The actual BFO/Carrier output is divided by 100 with U9 (to a nominal 455 KHz), low pass filtered, and applied to J7 BFO output, and J6 Carrier output.

(2) PLL Divider Element. The divider input is the VCO frequency and the output is always 1 KHz (loop locked). The programmable divider uses a prescaler/dual modulus technique with a PLL IC U5. The prescaler divides by 50 or by 51 (dual modulus, control line logic low = divide-by-11, logic high = divide-by-10)) thereby reducing the VCO input to a relatively low frequency for the programmable portion of the divider. The prescaler/dual modulus consists of U8 divide by 5, and U7, a dual modulus divide by 10/11. The U8 carry-out is strapped to U7 to develop the overall divide by 50/51 function. The programmable divider has counter A and counter N. The loading of the A and N counters are as follows:

Divide-by-N = BFO/CARRIER KHz Frequency x 2 (discard fraction)

Divide-by-A = BFO/CARRIER KHz - [Divide-by-N x 0.5] (ignore decimal)

(1) Example 1, BFO = 455.12 KHz

Divide-by-N = 455.12 x 2
= 910.24 (discard fraction)
= 910 (the Divide-by-N is loaded with "910")

Divide-by-A = 455.12 - [910 x 0.5]
= 455.12 - [455]
= .12 (ignore decimal)
= 12 (the Divide-by-A is loaded with "12")

(2) Example 2, BFO = 454.85 KHz

Divide-by-N = 454.85 x 2
= 909.7 (discard fraction)
= 909 (the Divide-by-N is loaded with "909")

Divide-by-A = 454.85 - [909 x 0.5]
= 454.85 - 454.5
= .35 (ignore decimal)
= 35 (the Divide-by-A is loaded with "35")

When the A counter counts down to zero during a divider cycle, its output is logic high commanding the dual modulus to change from divide by 51, to divide by 50. When the N counter counts down to zero during a divider cycle, its output is used to reload the A/N counters for another cycle, and provides an input to the phase detector element (see examples later in this section).

(3) PLL Divider Programming. The inputs to the A/N counters of PLL U5 are from microprocessor controlled parallel registers U1-U4. The registers U1/U2 are programmed with the carrier frequency (used during transmit), and registers U3/U4 are programmed with the BFO frequency (used during receive). The register outputs are enabled (logic high) by the CONDITIONED KEY PWB input via Q20 and inverter U10B. When the CONDITIONED KEY is logic low (transmitter keyed), the output of Q20 is logic high, and U1/U2 outputs are enabled. When the transmitter is unkeyed (receive), the output of Q20 is logic low, the output of U10B is logic high, and U3/U4 are enabled. The serial data and clock inputs to U1-U4 are from the MCB interface, however, the actual decoding for the register strobes is via the Synthesizer PWB MCB input circuit. Two of the

U1/U3 outputs are separate from the frequency programming. U1/U3-Q6 is used to enable the carrier/BFO outputs. When Q6 is a logic high, the carrier/BFO output is disabled. When Q6 is a logic low, the carrier/BFO output is enabled. U1/U3 output Q7 is used to enable the carrier/BFO BIT circuit. When Q7 is a logic high, the carrier/BFO BIT detector is disabled by turning on transistor Q23, which removes the dc bias from amplifier Q19.

(4) Phase detector element. The phase detector element is formed by digital outputs phase-R/phase-V with charge pump transistors Q11/Q12/Q13. When the PLL is locked, both phase-R/phase-V remain logic high, pulsing low for a very short duty cycle representing a small phase error. The logic outputs are buffered by double inversion with U6. During the logic low outputs of phase-R/phase-V (which varies in time, depending on the divider frequency), transistors Q11/Q12 form a current source and Q13 forms a current sink, developing a voltage across network C31, C32 and R53. The charge on C32 varies with the logic low time duration of phase-R/phase-V, hence the voltage at TP1 changes as the frequency changes, and the VCO control voltage is developed. The loop filter is passive and is formed by the C31/C32/R53 network. The final dc control voltage appears at VCO TP2.

b. Example of 455 KHz carrier generation. In the transmit mode, a carrier frequency is generated and used at the balanced modulator on the A1A1 Exciter PWB. In voice mode (AME, USB, LSB), the carrier frequency is exactly 455 KHz. The development of a transmit 455 KHz carrier frequency is as follows:

(1) For an output carrier frequency of 455 KHz, the VCO operates at 45.5 MHz. To generate 1 KHz from the divider element output (required for a phaselocked condition), the divider must operate at divide by 45,500, i.e., 45.5 MHz/45,500 = 1 KHz into the phase detector.

(2) The U1/U2 carrier frequency data registers are enabled with a CONDITIONED KEY input. The frequency information in the U1/U2 registers was previously entered by command from the A1A12 Control PWB, via the MCB. The frequency information then loads from the U1/U2 parallel outputs to the U5 A/N counter parallel inputs, coded in binary.

(3) For a carrier frequency of 455.00 KHz, the A counter information is "00", and the N counter information is "910" (see previous paragraphs for the calculation of the A and N divider characteristics).

(4) Since the N counter bits N5/N6 are tied to ground (logic 0) and the N counter bits N7/N8/N9 are tied to +5 Vdc (logic high), the range of numbers possible for the N counter are:

Hardwired					Programmed				
N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
1	1	1	0	0	0	0	0	0	0

= 896 (minimum)

-to-

Hardwired					Programmed				
N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
1	1	1	0	0	1	1	1	1	1

= 927 (maximum)

For this example, the N counter input is programmed for "910":

Hardwired					Programmed				
N9	N8	N7	N6	N5	N4	N3	N2	N1	N0
1	1	1	0	0	0	1	1	1	0

= 910

(5) The A counter has already commanded the dual modulus to divide by 50 (control line = logic high) since the A counter is at zero count. If the A counter was at any number besides zero, the dual modulus would be commanded to divide by 51 until the A counter counts down to zero.

(6) All of the preloading of the counters is accomplished after the last divider output, but before the arrival of the first input VCO pulse. The counter then begins to count VCO pulses. After 50 VCO sample pulses, the prescaler/dual modulus has an output. This reduces the N counter from 910 to 909. The next 50 VCO pulses are counted by the prescaler/dual modulus, and there is another output pulse. This reduces the N counter from 909 to 908. In this manner, the N counter is reduced to count 0 at which time it has an output pulse. At count 0, the A/N counters are reloaded and the cycle repeats. The total VCO pulses counted to yield one divider output pulse were: 50 VCO pulses x 910 = 45,500, i.e., the counter is dividing by the desired divisor of 45,500.

(7) The VCO frequency of 45.5 MHz is divided by 100 with U9 and the final carrier output frequency is the desired 45.5 MHz/100 = 455 KHz.

c. Example of 455 KHz BFO generation. When in the receive mode, a BFO frequency is generated and used at the product detector on the A1A7 Receive PWB. If operating in a SSB voice mode (USB, LSB, but not AME), the BFO frequency is exactly 455 KHz + offset. The development of a receive 455 KHz BFO frequency is as follows:

(1) For purposes of this example, assume the operator has selected the LSB mode of operation with a negative BFO offset of 120 Hz. Since the transceiver frequency scheme reverses the USB and LSB sidebands, the audio frequencies associated with LSB are above the center frequency of 455 KHz. Therefore, to enter a negative BFO frequency, i.e., a frequency that will lower the audio frequency output of the product detector, the 455 KHz BFO is raised above 455 KHz by the offset amount. So, for this example, the desired BFO frequency is 455.120 KHz.

(2) For an output BFO frequency of 455.120 KHz, the VCO will be operating at 45.512 MHz. To generate 1 KHz from the divider element output (required for a phaselocked condition), the divider must operate at divide by 45,512, i.e., 45.512 MHz/45,512 = 1 KHz into the phase detector.

(3) The U3/U4 BFO frequency data registers are enabled with an inverted CONDITIONED KEY input, via inverter U10B. The frequency information in the U3/U4 registers was previously entered by command from the A1A12 Control PWB, via the MCB. The frequency information then loads from the U3/U4 parallel outputs to the U5 A/N counter parallel inputs, coded in binary.

(4) For a BFO frequency of 455.120 KHz, the A counter information is "12", and the N counter information is "910". See previous paragraphs for the calculation of the A and N divider characteristics.

(5) Since the N counter bits N5/N6 are tied to ground (logic 0) and the N counter bits N7/N8/N9 are tied to +5 Vdc (logic high), the range of numbers possible for the N counter is:

```
|--  Hardwired   -| |-  Programmed  -|
N9 N8 N7 N6 N5   N4 N3 N2 N1 N0
 1  1  1  0  0   0  0  0  0  0
```

= 896 (minimum)

-to-

```
|--  Hardwired   -| |-  Programmed  -|
N9 N8 N7 N6 N5   N4 N3 N2 N1 N0
 1  1  1  0  0   1  1  1  1  1
```

= 927 (maximum)

For this example, the N counter input is programmed for "910":

```
|--  Hardwired   -| |-  Programmed  -|
N9 N8 N7 N6 N5   N4 N3 N2 N1 N0
 1  1  1  0  0   0  1  1  1  0
```

= 910

(6) None of the A counter bits are hardwired; therefore, for the 6-bit binary A counter inputs, the maximum and minimum counts are:

```
|----Programmed-----|
A5 A4 A3 A2 A1 A0
 0  0  0  0  0  0
```

= 0 (minimum))

-or-

```
|----Programmed-----|
A5 A4 A3 A2 A1 A0
 1  1  1  1  1  1
```

= 63 (maximum)

For this example, the input is programmed for "12":

```
|----Programmed-----|
A5 A4 A3 A2 A1 A0
 0  0  1  1  0  0
```

= 12

(7) All of the preloading of the counters is accomplished after the last divider output, but before the arrival of the first input VCO pulse. The counter then begins to count VCO pulses. Since the A counter is not at zero, the dual modulus control line is

set for divide by 51 (control line = logic low). After 51 VCO sample pulses, the prescaler/dual modulus has an output. This reduces the N counter from 910 to 909, and the A counter from 12 to 11. The next 51 VCO pulses are counted by the prescaler/dual modulus, and there is another output pulse. This reduces the N counter from 909 to 908, and the A counter from 11 to 10. In this manner, the A counter is reduced to count 0 at which time the dual modulus control line changes from divide by 51 (control line = logic low), to divide by 50 (control line = logic high).

(8) When the A counter arrived at zero, a total of 51 VCO pulses x 12 = 612 VCO pulses had been counted. The N counter status stands at 910 - 12 = 898, and the dual modulus is now set at divide by 50 (control line = logic high) for the remainder of the divider cycle. The next 50 VCO pulses are counted, and the N counter goes to 897, etc. Once the dual modulus is set to divide by 50, it requires 50 VCO pulses x 898 = 44,900 more VCO pulses to count down the N counter and get a divider N output. At N counter count 0, the A/N counters are reloaded and the cycle repeats.

(9) For each complete divider cycle, it requires 612 VCO pulses to count down the A counter, and an additional 44,900 pulses to finish counting down the N counter, for a total of 612 + 44,900 = 45,512 VCO pulses total for a divider output. Therefore, the divider is operating at a divisor of 45,512, i.e., the desired divider characteristic.

(10) The VCO frequency of 45.512 MHz is divided by 100 with U9 and the final BFO output frequency is the desired 45.512 MHz/100 = 455.12 KHz.

d. Reference/BFO PWB BIT detectors. Unlike many of the transceiver assemblies, the Reference/BFO PWB BIT output is logic high for a successful BIT and logic low for a failed BIT. When the Reference/BFO PWB is exercised during BIT testing, four BIT detectors are operating:

(1) BFO/Carrier PLL unlock detector. When the BFO/Carrier loop is locked, the PLL IC U5-28 has a logic high output. If the PLL is not locked, the U5-28 pulses low. Transistor Q7, with an integrator network at the base input, is used to detect the unlocked condition. As the low pulses are applied to C26, the capacitor is discharged and Q7 is turned on. This places a +5 Vdc signal at the collector of Q7, turning on transistors Q8 and Q9. The Q9 transistor is used to signal the Control PWB of the unlocked condition through the RF ATTENTION logic low, and the Q8 transistor is used to signal a BIT failure by a logic low output.

(2) 1 KHz audio signal detector. The 1 KHz signal is detected by CR18 which turns on transistor Q10. With Q10 turned on, diode CR27 does not conduct. Therefore, transistor Q6 is not turned on and transistor Q8 is not turned on. The diodes tied to the base of Q6 must all go to a logic high condition if BIT is successful. If any of the three diodes start to conduct due to a detected low, transistor Q6 will turn on, transistor Q8 will turn on and a logic low will be applied at the BIT output indicating BIT failed.

(3) 40 MHz 2nd LO detector. The 40 MHz output line is sampled and amplified by transistors Q3 and Q4. The output of Q4 is rectified and filtered into a +dc voltage. This is tied to diode CR17 which will not conduct when the 40 MHz is detected. If the 40 MHz is not present, CR17 will conduct, transistor Q6 will turn on, transistor Q8 will turn on and a logic low will be applied at the BIT output indicating BIT failed.

(4) 455 KHz detector. The 455 KHz BFO/Carrier output is sampled and amplified by Q18 and Q19. The output of Q19 is rectified by CR21/CR22 and filtered by C75. The +dc output will prevent CR23 from conducting when the 455 KHz BFO/Carrier output is detected. If the 455 KHz is not present, CR23 will conduct, transistor Q6 will turn on, transistor Q8 will turn on and a logic low will be applied at the BIT output indicating BIT failed. If the carrier/BFO BIT detector is disabled by a logic high at U1/U3-Q7, CR23 will not conduct due to the (approximately) +5 V applied to the cathode of CR23 via R87 from U1/U3-Q7.

5-53. SYNTHESIZER PWB ASSEMBLY A1A10, 10085-5600. This manual portion describes the Synthesizer PWB as an individual assembly. Section I of this chapter describes the function of the Synthesizer PWB in relation to overall transceiver operation. The following references apply to the detailed discussion that follows:

a. Simplified Synthesizer Block Diagram	Figure 5-13
b. Simplified Synthesizer Phase Detector	Figure 5-14

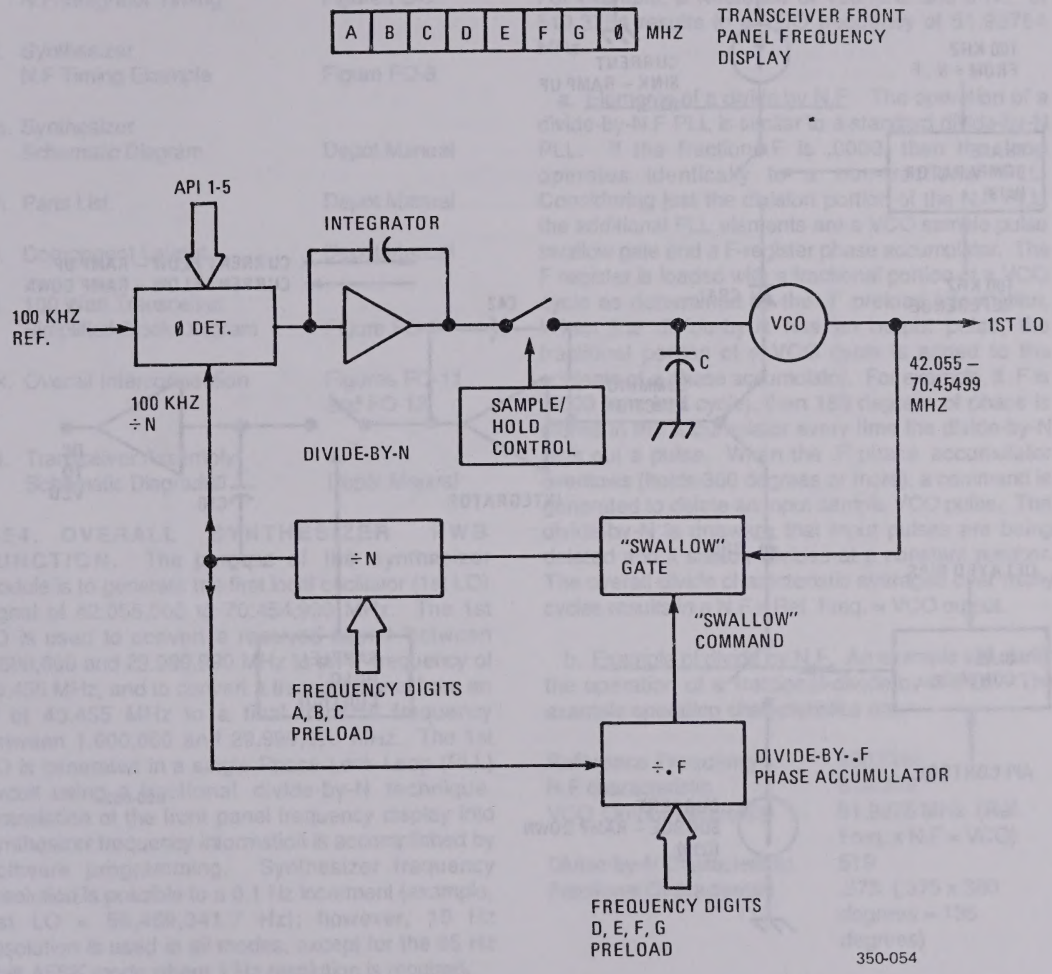


Figure 5-13. Synthesizer Simplified Block Diagram

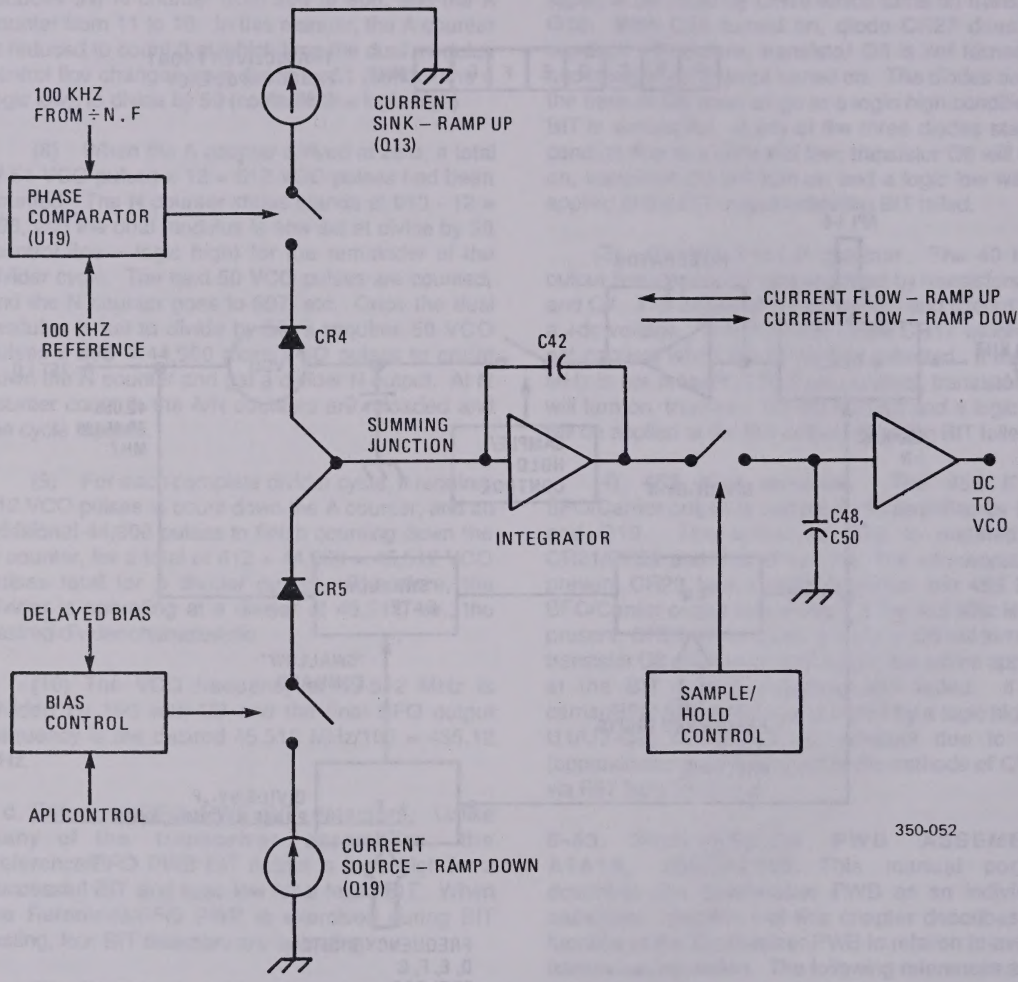


Figure 5-14. Synthesizer Simplified Phase Detector Operation

c. Synthesizer Integrator Output	Figure 5-15
d. Simplified Synthesizer Divide-by-N	Figure 5-16
e. Synthesizer N.F/Integrator Timing	Figure FO-7
f. Synthesizer N.F Timing Example	Figure FO-8
g. Synthesizer Schematic Diagram	Depot Manual
h. Parts List	Depot Manual
i. Component Layout	Depot Manual
j. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
k. Overall Interconnection	Figures FO-11 and FO-12
l. Transceiver Assembly Schematic Diagrams	Depot Manual

5-54. OVERALL SYNTHESIZER PWB FUNCTION. The purpose of the synthesizer module is to generate the first local oscillator (1st LO) signal of 42.055,000 to 70.454,990 MHz. The 1st LO is used to convert a received signal between 1.600,000 and 29.999,990 MHz to an IF frequency of 40.455 MHz, and to convert a transmit signal from an IF of 40.455 MHz to a final transmit frequency between 1.600,000 and 29.999,990 MHz. The 1st LO is generated in a single Phase Lock Loop (PLL) circuit using a fractional divide-by-N technique. Translation of the front panel frequency display into synthesizer frequency information is accomplished by software programming. Synthesizer frequency resolution is possible to a 0.1 Hz increment (example, 1st LO = 56,469,341.7 Hz); however, 10 Hz resolution is used in all modes, except for the 85 Hz shift AFSK mode where 1 Hz resolution is required.

5-55. DESCRIPTION OF FRACTIONAL DIVIDE-BY-N PHASE LOCK LOOP. A simplified block diagram of Synthesizer operation is shown in figure 5-13. In a non-fractional phaselock loop (PLL), the output frequency of the loop is: F ref. x Divide-by-N. For example, if the reference is 100 KHz and the divide-by-N is 519 , the VCO frequency is 51.9 MHz. The frequency resolution of the PLL is 100 KHz since the divide-by-N can only be an integer. A fractional divide-by-N phase lock loop can generate a frequency output with a frequency resolution much finer than the PLL phase detector reference frequency. As in a standard PLL, the VCO output frequency is F Ref x divide-by-N.F (number fraction). For example, a reference of 100 KHz and a N.F of 519.3754 results in a VCO frequency of 51.93754 MHz.

a. Elements of a divide by N.F. The operation of a divide-by-N.F PLL is similar to a standard divide-by-N PLL. If the fraction .F is .0000, then the loop operates identically to a non-fractional PLL. Considering just the division portion of the N.F PLL, the additional PLL elements are a VCO sample pulse swallow gate and a F-register phase accumulator. The F register is loaded with a fractional portion of a VCO cycle as determined by the .F preload information. When the divide-by-N has an output pulse, the fractional portion of a VCO cycle is added to the contents of a phase accumulator. For example, if .F is .5000 (one half cycle), then 180 degrees of phase is stored in the accumulator every time the divide-by-N puts out a pulse. When the .F phase accumulator overflows (holds 360 degrees or more), a command is generated to delete an input sample VCO pulse. The divide-by-N is unaware that input pulses are being deleted and it steadly divides at a constant number. The overall divide characteristic averaged over many cycles results in a N.F x Ref. Freq. = VCO output.

b. Example of divide by N.F. An example will clarify the operation of a fractional-divide-by-N PLL. The example operating characteristics are:

Reference Frequency	100 KHz
N.F characteristic	519.375
VCO Output frequency	51.9375 MHz (Ref. Freq. x N.F = VCO)
Divide-by-N Characteristic	519
Fractional Characteristic.	.375 (.375 x 360 degrees = 135 degrees)

Note

The fractional characteristic should be considered in fractions of a VCO cycle rather than in degrees of a VCO cycle, i.e., .375 of phase accumulation rather than 135 degrees of accumulation.

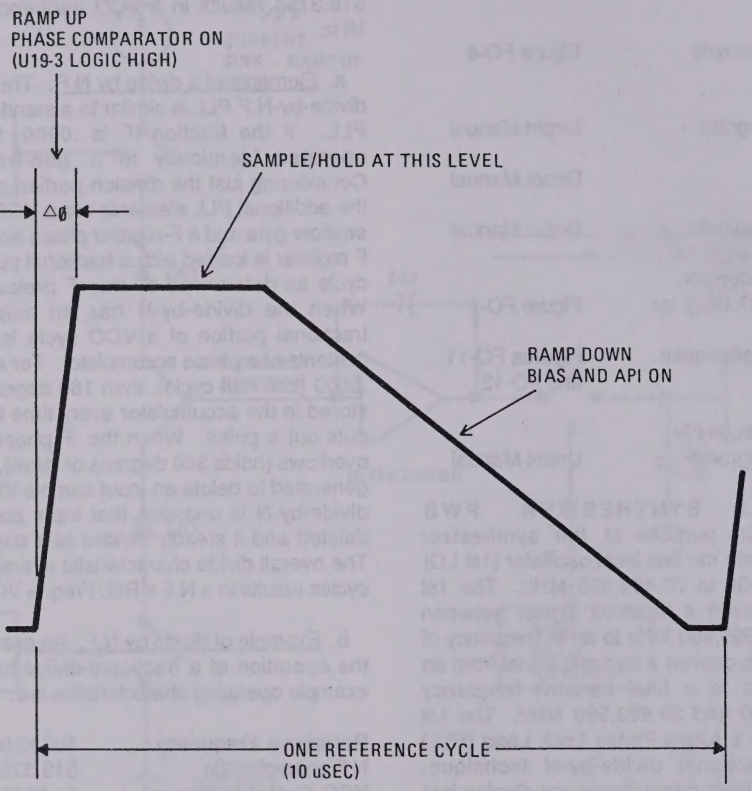


Figure 5-15. Synthesizer Simplified Integrator Waveform

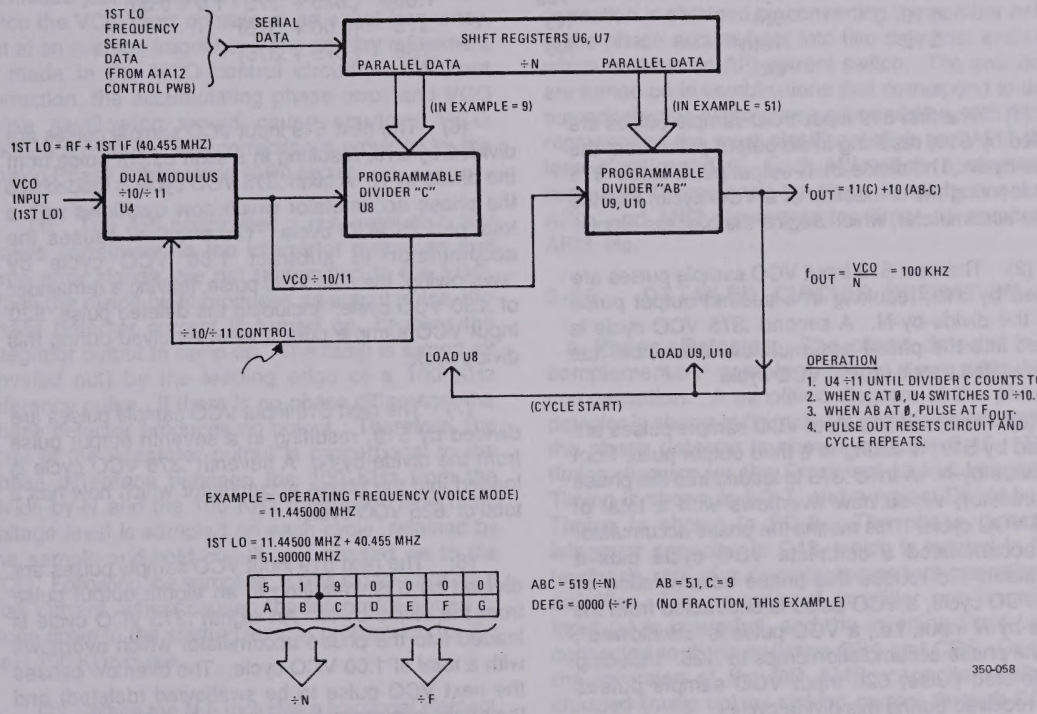

1ST LO FREQUENCY SERIAL DATA (FROM A1A12 CONTROL PWB)
SERIAL DATA
SHIFT REGISTERS U6, U7
PARALLEL DATA
÷N
PARALLEL DATA
(IN EXAMPLE = 9)
(IN EXAMPLE = 51)
1ST LO = RF + 1ST IF (40.455 MHZ)
VCO INPUT (1ST LO)
DUAL MODULUS ÷10/÷11 U4
PROGRAMMABLE DIVIDER "C" U8
PROGRAMMABLE DIVIDER "AB" U9, U10
fOUT = 11(C) +10 (AB-C)
fOUT = VCO/N = 100 KHZ
VCO ÷ 10/11
÷10/÷11 CONTROL
LOAD U8
LOAD U9, U10
(CYCLE START)
OPERATION
1. U4 ÷11 UNTIL DIVIDER C COUNTS TO Ø.
2. WHEN C AT Ø, U4 SWITCHES TO ÷10.
3. WHEN AB AT Ø, PULSE AT FOUT.
4. PULSE OUT RESETS CIRCUIT AND CYCLE REPEATS.
EXAMPLE – OPERATING FREQUENCY (VOICE MODE) = 11.445000 MHZ
1ST LO = 11.44500 MHZ + 40.455 MHZ = 51.90000 MHZ
5 1 9 0 0 0 0
A B C D E F G
ABC = 519 (÷N)
DEFG = 0000 (÷F)
AB = 51, C = 9
(NO FRACTION, THIS EXAMPLE)
÷N
÷F
350-058

Figure 5-16. Synthesizer Simplified Divide by N Diagram

Note

For voice modes of operation, the 1st LO is equal to the operating frequency plus 40.455 MHz. Therefore, for this example, the transceiver would be operating at a frequency of 11.4825 MHz.

VCO Pulses In	Divide Out	Swallow?	Phase Accumulation	
519	1st	No	.375	(0.00 + .375)
519	2nd	No	.750	(.375 + .375)
520	3rd	Yes	1.125	(.750 + .375 - 1.0 = .125)
519	4th	No	.500	(.125 + .375)
519	5th	No	.875	(.500 + .375)
520	6th	Yes	1.250	(.875 + .375 - 1.0 = .250)
519	7th	No	.625	(.250 + .375)
520	8yh	Yes	1.000	(.625 + .375 - 1.0 = 0.00)
519	9th	No	.375	(0.00 + .375)
519	10th	No	.750	(.375 + .375)
	etc.			

(1) The first 519 input VCO sample pulses are divided by 519, resulting in an output pulse from the divide-by-N. The divide-by-N output pulse loads .375 (representing the .F fraction of a VCO cycle) into the phase accumulator, which begins the process empty.

(2) The next 519 input VCO sample pulses are divided by 519, resulting in a second output pulse from the divide-by-N. A second .375 VCO cycle is loaded into the phase accumulator, which now has accumulated a total of .750 VCO cycle.

(3) The next 519 input VCO sample pulses are divided by 519, resulting in a third output pulse from the divide-by-N. A third .375 is loaded into the phase accumulator, which now overflows with a total of 1.125 VCO cycle. This means the phase accumulator has accumulated a complete VCO cycle plus a remainder. To reduce this phase accumulation by 1.00 VCO cycle, a VCO pulse is subtracted from the divide-by-N input, i.e., a VCO pulse is "swallowed", and the phase accumulation drops to .125. Including the deleted pulse, 520 input VCO sample pulses were received during this divide cycle.

(4) The next 519 input VCO sample pulses are divided by 519, resulting in a fourth output pulse from the divide-by-N. A fourth .375 VCO cycle is loaded into the phase accumulator, which now has a total of .500 VCO cycle.

(5) The next 519 input VCO sample pulses are divided by 519, resulting in a fifth output pulse from the divide-by-N. A fifth .375 VCO cycle is loaded into the phase accumulator which now has a total of .875 VCO cycle.

(6) The next 519 input VCO sample pulses are divided by 519, resulting in a sixth output pulse from the divide-by-N. A sixth .375 VCO cycle is loaded into the phase accumulator which now overflows with a total of 1.25 VCO cycle. The overflow causes the accumulator to subtract 1.00 VCO cycle by "swallowing" the next VCO pulse, leaving a remainder of .250 VCO cycle. Including the deleted pulse, 520 input VCO sample pulses were received during this divide cycle.

(7) The next 519 input VCO sample pulses are divided by 519, resulting in a seventh output pulse from the divide-by-N. A seventh .375 VCO cycle is loaded into the phase accumulator which now has a total of .625 VCO cycle.

(8) The next 519 input VCO sample pulses are divided by 519, resulting in an eighth output pulse from the divide-by-N. An eighth .375 VCO cycle is loaded into the phase accumulator which overflows with a total of 1.00 VCO cycle. The overflow causes the next VCO pulse to be swallowed (deleted) and the phase accumulator is empty with 0.00 VCO cycle. Including the deleted pulse, a total of 520 input VCO sample pulses were received during this divide cycle.

(9) With the accumulator empty, the cycle now repeats for each 8 divide-by-N output pulses. To calculate the average divide number for this example:

Total VCO pulses: 519 + 519 + 520 + 519 + 519 + 520 + 519 + 520 = 4155

Divider output pulses: 8

Average divider characteristic	4155/8 = 519.375
VCO Frequency	= Reference Frequency x divider characteristic
	= 100 KHz x 519.375
	= 51.9375 MHz, the desired VCO frequency

c. Analog Phase Interpolation. The divide-by-N.F technique just described requires some refinement since the VCO must operate at an exact frequency, not at an average frequency. The primary refinement is made in the VCO control circuitry. Without correction, the accumulating phase error and VCO pulse swallowing would cause spurious VCO frequency outputs. The correction is provided by the Analog Phase Interpolation (API) circuit.

(1) The API anticipates a pulse deletion and makes corrections to the integrator output so that large error signals are not transmitted to the VCO. When the divide-by-N produces an output pulse, the phase detector current is turned on, causing the integrator output to ramp up. The ramp is turned off (leveled out) by the leading edge of a 100 KHz reference pulse. If there is no phase difference, the phase detector produces no output. Therefore, the level of the integrator output is proportional to the phase difference between the 100 KHz from the divide-by-N and the 100 KHz reference. The ramp voltage level is sampled on each cycle, retained by the sample-and-hold circuit and passed on to the VCO. Following the sampling, a bias signal turns on a bias current, which causes the integrator output to slope down to the starting level in preparation for the next 100 KHz pulse.

(2) When the N.F includes a fractional element, the VCO operates at a frequency somewhat higher than the divide-by-N indicates. In the example, the divide-by-N is 519, indicating a VCO frequency of 51.9 MHz, where the actual VCO frequency due to the .F fraction is 51.9375 MHz. The fractional part of the VCO frequency causes the integrator to reach a higher output peak on each succeeding reference cycle as the phase difference accumulates. The API compensates for this by commanding the bias signal to start below the previous starting level for each succeeding cycle. In this way, the integrator always ramps up to the same level. The sample is taken at the same level each time and the VCO control voltage is steady at the exact level required to obtain the correct VCO frequency.

(3) The ramp-down current is controlled by five API switches, which are in turn controlled by the phase accumulator. Each time the divide-by-N produces an output pulse, the phase accumulator is incremented with the phase characteristic (.375 VCO cycle in the example above). The number stored in the phase accumulator at any time corresponds to the accumulated phase difference. The 100 KHz divide-by-N sample pulses occur sooner and sooner with reference to the 100 KHz reference pulse. The correction is obtained by converting the number held in the phase accumulator into five data bits, each of which controls an API current switch. The switches are turned on in combinations that correspond to the numerical value of the phase accumulation, with API1 representing the most significant digit and API5 the least significant digit. Each API switch represents a current. API1 represents ten times as much current as API2, and API2 represents ten times as much as API3, etc.

5-56. DETAILED CIRCUIT OPERATION.

a. Phase Detector. The phase detector is a complementary sample-and-hold type with API compensation. A simplified diagram of the phase detector is shown in figure 5-14, and the waveform for the phase detector is shown in figure 5-15. The timing diagram for the Fractional N and Integrator Timing is shown in FO-7, and a typical Divide by N Timing is shown in FO-8. The phase detector integrator capacitor is C42, which is located in the feedback path of a discrete component operational amplifier. The operational amplifier non-inverting input (+) is grounded, and the inverting input (-) is connected to diode switches CR4 and CR5. Due to the inversion of the OP AMP, capacitor C42 is charged (ramp up) by sinking current through CR4. Capacitor C42 is discharged (ramp down) through CR5 by a current source. The duration of the up ramp is determined by the total static and differential phase difference between the divide-by-N input and the 100 KHz reference input. After ramp up, the ramp levels off and the voltage on C42 is sampled. It is this dc voltage that controls the VCO at the exact frequency required for phase lock.

(1) After sampling, the down ramp period occurs. The down ramp time duration is fixed, and the ramp slope varies depending on the content of the phase accumulator. It is during the down ramp period

that phase detector compensation is accomplished. Depending on the API input, which represents the phase accumulation, the down ramp current is adjusted so that the next up ramp will terminate at exactly the same dc level as the previous sample. If the up ramp reaches a level higher than the previous up ramp, then the down ramp goes lower in compensation. The magnitude of the up ramp current is approximately ten times the down ramp current, which accounts for the steep up ramp and the less steep down ramp.

(2) If the N.F characteristic has no .F (fractional) component, the up ramp and down ramp are at the same level for each divide-by-N output. With a fractional component, the accumulating phase error increases the charging time for C42 and the dc level at TP2 increases, and must be compensated for by the API correction as discussed above.

b. Phase detector up ramp and sample. The timing for the up ramp of the sample-and-hold waveform is generated by phase comparator flip-flop U19. The U19 device uses emitter coupled logic (ECL). A logic high is a minimum of +4.0 volts, and a logic low is a maximum of +3.4 volts. The inputs to U19 are the 100 KHz divide-by-N and the 100 KHz reference. The 100 KHz reference comes from divide-by-2 flip-flop U17A (the input reference to the board is 200 KHz) and shaping network associated with transistor Q4. The resultant 100 KHz reference is a sharp, fast-rising pulse. When U19A-3 goes logic high, indicating the arrival of a VCO N.F pulse, transistor Q41 turns off and transistor Q7 turns on. With Q7 turned on, the anode of CR3 is pulled below ground and turns off. Effectively, CR3 is removed from the circuit, and a current path is established from the output of the discrete component operational amplifier (TP2), through integrator capacitor C42 and diode CR4, to the current sink via Q13. As the capacitor charges, the +dc voltage at TP2 increases. The up ramp stops when the 100 KHz reference pulse arrives at U19B-11, which reverses the switching sequence of Q41 and Q7. With Q7 off and Q6 on, a positive voltage appears at the anode of CR3, turning on the diode and reverse biasing CR4, i.e., the current sink is removed and the capacitor can no longer charge. With no current flowing in any direction through the capacitor, the voltage held by the capacitor remains steady and can be sampled.

c. Phase detector down ramp. The down ramp of C42 starts with a logic high TTL DELAYED BIAS command applied to transistor Q8. Q8 then turns on, which turns off transistor Q9. With Q9 turned off, CR12 is effectively removed from the circuit and current is allowed to flow through diode CR5. The amount of current flowing depends on how many of the API logic inputs are set. If there is no API control (no fractional .F), then all the API current sinks are enabled, reducing the amount of current through CR5. As the API control lines are active (logic high), the API current sinks are removed and the current through CR5 increases. With the increased current, the down ramp is greater than the previous down ramp, and the API correction is accomplished for the divide-by-N output.

(1) The current sink path for API1 is controlled by transistor Q11. Q11 is turned on when the delayed bias control signal is present (logic high). Selection of API1 (logic high) turns on transistor Q12, which reverse biases diode CR6 and the current sink path is disabled. More current is supplied for the down ramp. Operation of the other API lines is similar, with a control voltage disabling the current sink for each associated control line.

(2) At the end of the DELAYED BIAS duration, (13 VCO divide-by-10 pulses), a reverse switching sequence with Q8/Q9 occurs, and the down ramp sequence is completed. The actual down ramp time varies since it is fixed at 13 VCO cycles/10, and the VCO frequency varies from approximately 40 to 70 MHz.

d. Sample and hold. Sample and hold FET switches Q23 and Q24 operate simultaneously with the control input SAMPLE/HOLD CONTROL. The integrator plateau is sampled directly by Q23 with the voltage held on capacitor C48. At the same time, the voltage on C48 is sampled by Q24 and stored on capacitor C50. The two-stage sample circuit reduces any ripple that may be present in the ramp plateau. The voltage on C50 is amplified by unity gain FET buffer amplifier AR2. The high input impedance of AR2 assures minimum load on the voltage held by C50. The final VCO dc voltage, reflected at TP3, is applied to the passive loop filter and VCO tuning diodes.

e. VCO. The VCO consists of a set of varactor diodes connected to a +12 Vdc voltage reference. The control voltage applied to the varactors changes the capacitance of the devices, and therefore, the frequency of the VCO. Oscillator transistor Q1 operates in conjunction with feedback transformer T1. A small secondary winding of T1 is used to tap

the final VCO frequency. The VCO output is processed by two amplifier circuits. One output exits the PWB as the 1st LO and the other output is used as the VCO sample for PLL divider circuits, after buffering by transistor Q4.

f. Divide by N.F Circuit. The elements of the divide by N circuit are a dual modulus prescaler U4 (divide by 10/11); two blocks of programmable dividers, U8, U9, and U10; and a LSI fractional gate array U5. The divide by .F is processed in the U5 Fractional N Logic Array to keep track of the fractional component in the phase accumulator, and generate the timing for the VCO pulse swallow command. The N programmable dividers are loaded with numeric information from the first three significant digits of the 1st LO frequency, and the .F dividers are loaded with numeric information from the last four significant digits. The 1st LO frequency = RF + 1st IF (40.455 MHz). The 100 Watt Transceiver operates over an RF frequency range of 1.600,000 to 29.999,990 MHz, so that the range of the 1st LO is 42.055 to 70.45499 MHz. Therefore, the first three significant digits of the 1st LO range from 420 to 704 for the divide by N, and the remaining digits 0000 to 9999 are used for the divide by .F.

g. Divide by N.

(1) As shown in figure 5-16, the 1st LO digits are in the order ABCDEFG. For example:

	AB CDEFG	
1st LO	42.05500	MHz
1st LO	70.45499	MHz

The digits ABC are used in the divide by N circuit, and the remaining digits DEFG are used in the fractional divide by .F circuit. Operation of the divide by N circuit is the same with or without a .F component. The divide by N simply considers the ABC digit information and divides accordingly with the dual modulus prescaler and two blocks of programmable dividers.

(2) The U8 divide by N programmable block is preloaded with "C" information, and U10 and U9 are preloaded with "AB" information respectively. The "C" divider can be any number between 0-9, and the "AB" divider can be any number between 42 to 70. During the division cycle, the preloaded dividers both count down to "0". When this occurs, the input VCO frequency sample is divided exactly by a number that yields a divider output frequency of 100 KHz. The dual modulus prescaler U4 prescales the VCO frequency and supplies a programmable division characteristic of divide by 10 or divide by 11.

(3) At the start of a division cycle, dual modulus prescaler U4 divides by 11. Therefore, for every 11 VCO input pulses, there is 1 dual modulus output pulse. Each dual modulus output pulse counts down the preloaded number in both the "AB" and "C" programmable dividers. This continues until the "C" counter has counted down to zero and sends a RIPPLE CARRY OUT (RCO) pulse to the dual modulus prescaler. The RCO pulse disables the "C" divider from further counting and programs the dual modulus prescaler to now divide by 10, instead of 11. The VCO division continues with each group of 10 VCO input pulses, yielding 1 prescaler output pulse, which counts the "AB" programmable divider down one more step toward zero. When the programmable divider "AB" reaches zero, a new cycle is started and the entire process is repeated.

(4) An example will clarify the operation of the divide-by-N circuit. The parameters for this example are:

Transceiver Mode of Operation:	USB
Transceiver Frequency of Operation:	11.445000 MHz

Note:

A voice mode of operation is assumed because the 1st LO is offset in the CW and AFSK modes.

1st LO frequency = RF + 1st IF (40.455 MHz)
= 11.445000 MHz + 40.455 MHz
= 51.90000 MHz

Reference
A B C D E F G
5 1 . 9 0 0 0 0 MHz

ABC is the divide by N portion, i.e., divide by 519. The divide by .F portion, DEFG, is 0000; therefore, there is no fractional .F component. The divide by 519 must now divide the VCO frequency (1st LO) of 51.90000 MHz to yield the desired 100 KHz output.

h. Events for one divide by 519 cycle.

(1) The transceiver operating frequency is 11.44500 MHz. The A1A12 Control PWB processes this information and writes the corresponding 1st LO frequency of 51.9 MHz into the A1A10 Synthesizer

PWB via the Module Control Bus (MCB). The MCB address and strobes are decoded by U1.

(2) The serial digital data, coded with the 1st LO 51.9 MHz frequency information, is clocked into serial-to-parallel registers U6 and U7 after processing by U5. Q45 strobes U6/U7 and the data appears at the parallel outputs.

(3) Between the last divider output pulse and the next VCO pulse, the programmable dividers U8, U9, U10, are preloaded by a CYCLE START command. The "9" of the divide by 519 is loaded in the U8 "C" divider, and the "51" of the divide by 519 is loaded in the U10, U9 "AB" divider.

(4) At the start of this (and every) divider cycle, the dual modulus prescaler U4 is programmed for divide by 11. Therefore, after the first 11 input VCO pulses, a prescaler output pulse steps down the C divider from 9 to 8, and the AB divider from 51 to 50. In this same manner, after another 88 input VCO pulses, the C divider has stepped to 0, and the AB divider has stepped to 42. Overall, 99 input VCO pulses occur in this part of the cycle.

(5) When the C divider reaches 0, a U8 RIPPLE CARRY OUT (RCO) pulse from the C divider stops further C divider counting, and causes the dual modulus prescaler to be commanded to divide by 10 (instead of 11).

(6) After another 10 input VCO pulses, the prescaler produces an output pulse, and the AB divider steps from 42 to 41. After another 10 input VCO pulses, the A13 divider steps from 41 to 40, and so forth. Overall, the prescaler requires 420 input VCO pulses to step the AB divider from 42 to 0.

(7) When the U9/U10 AB counter reaches a count of one, a logic low occurs at U11-6. This pulse is used to preload the AB dividers and is named CYCLE START. The next rising clock edge from the prescaler loads the C divider (U8) and the AB divider (U9, U10), and the divide by 519 cycle repeats.

(8) The total VCO pulses required for 1 divider output including 99 for the C divider count down, plus 420 for the rest of the AB divider count down, total 519; thus, the circuit operates at the desired divide-by-519.

(9) Although the CYCLE START output operates at 100 KHz, it is not used as the 100 KHz divide-by-N sample. Instead, CYCLE START is processed in Fractional N Logic Array U5 to generate the API, bias, swallow, sample, and API Latch Clock signals. The 100 KHz sample is derived from processing the bias and delayed bias outputs of U5, which are then converted into a fast-rising pulse by flip-flop U16 and transistor Q3.

i. Divide by .F (Fractional).

(1) The fractional portion of the divide by N.F. functions in relation to the divider circuit by deleting or "swallowing" an input VCO pulse. This has the effect of removing 1 cycle, or 360 degrees, of phase accumulation as previously described. The divide-by-N is unaffected by the action of the divide-by-.F, and the circuits essentially operate independently. Virtually all of the divide-by-.F functions are processed internally to LSI integrated circuit U5. Since a discussion of the internal workings of U5 is beyond the scope of this manual, only the divide by .F outputs are considered: API control, bias, and swallow control.

(2) The operation of the API control is discussed in the phase detector circuit description, as is the bias control. The swallow control is interactive with the dual modulus divider used with the divide by N circuit. The dual modulus divider U4 (divide-by-10 or 11) is operating as a divide-by-11 until the preloaded "C" divider underflows by counting down to zero. At that time, the dual modulus is programmed to divide by 10 for the remainder of the divide-by-N cycle. The divide-by-.F VCO pulse swallow occurs by changing the dual modulus divider from divide-by-10, back to divide-by-11 for one VCO pulse, and then back to divide-by-10 again. In this manner, a prescaler output counts down the AB divider one step with 11 VCO pulses, instead of 10 VCO pulses, and a VCO pulse is thereby swallowed.

(3) The swallow command may be generated during the first 10 cycles of the VCO/10 or 11 output. This means that the C divider counts down from its preload during the same time a swallow command may occur. If the swallow command occurs when the dual modulus divider is already dividing by 11, or if a swallow command occurs at the same time the C divider underflows, the swallow command must be "stored" until the proper time. This is accomplished by using the swallow control flip-flop U18.

j. Module Control Bus (MCB) Interface.

(1) The control signals for the Synthesizer PWB are read into the assembly in a serial data stream. The MCB address strobe is decoded for both the Synthesizer PWB and Reference/BFO PWB. The RF ADD3/RF ADD2/RF ADD1/RF ADD0 address for the Synthesizer PWB is 0000 (0); for the transmit carrier frequency generated on the REF/BFO PWB, the address is 1000 (8); and for the BFO frequency, the address is 0100 (4). Both Read and Write are decoded for the Synthesizer PWB; only the Write functions are decoded for the Reference/BFO PWB (carrier and BFO frequencies). RF ADD1 and RF ADD0 are used as enables for 1-of-8 decoder U1, and RF ADD3 and RF ADD2 are used as decoder inputs along with the read/write strobe.

(2) When MCB data is intended for the synthesizer PWB, the decoding generates the desired enables for the bus registers. The clock signal then clocks serial bits of data into the U5 shift register port. The first data bit to enter is stored in the last bus register port and is used as part of the synthesizer MCB loop back BIT test sequence (Q8 output of register U7). After all data is clocked in, the "write" strobe is decoded and the data in the bus registers is latched into the bus storage registers and appears at the bus register output pins as steady control voltages.

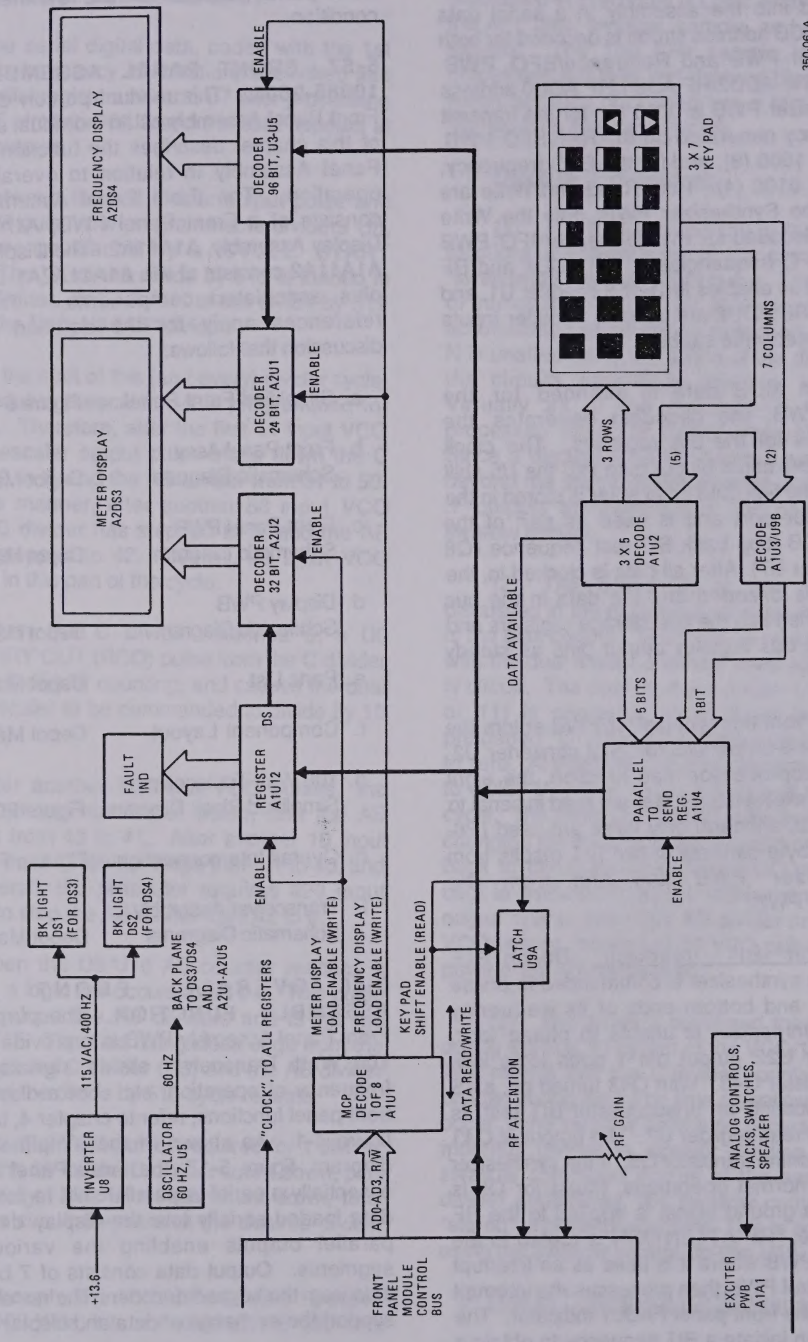
(3) Data from the synthesizer PWB enters the control PWB via 8-bit parallel-to-serial converter U2. During the microprocessor read function, the eight inputs to the parallel/serial register are read in serial to the Control PWB, although only three are used (P6-P8). The 8-bit byte consists of two BIT results from the Synthesizer PWB and one from the Reference/BFO PWB.

k. Synthesizer BIT Interface. During BIT sequencing, the synthesizer is commanded to phase lock at the top and bottom ends of its frequency range. If the synthesizer is unable to phase lock, unlock detector U22 output pin 1 goes logic low, turning on transistor Q43. With Q43 turned on, a +5 Vdc signal, indicating an unsuccessful BIT test, is sent to the MCB read register U2. The output of Q43 is also used to control transistor Q5. If the synthesizer unlocks during normal operations, transistor Q5 is turned on and a ground signal is applied to the RF ATTENTION line. RF ATTENTION is routed to the A1A12 Control PWB where it is used as an interrupt signal. The Control PWB then processes the interrupt and illuminates the front panel FAULT indicator. The operator can then initiate a BIT sequence to obtain a front panel readout of the synthesizer unlock condition.

5-57. FRONT PANEL ASSEMBLY A1A11, 10085-2000. This manual portion describes the Front Panel Assembly as an individual unit. Section I of this chapter describes the function of the Front Panel Assembly in relation to overall transceiver operation. The Front Panel Assembly, A1A11, consists of a Front Panel PWB, A1A11A1, and a Display Assembly, A1A11A2. The Display Assembly, A1A11A2 consists of the A1A11A2A1 Display PWB, plus associated components. The following references apply for the detailed Front Panel discussion that follows:

a. Simplified Front Panel	Figure 5-17
b. Front Panel Assy Schematic Diagram	Depot Manual
c. Front Panel PWB Schematic Diagram	Depot Manual
d. Display PWB Schematic Diagram	Depot Manual
e. Parts List	Depot Manual
f. Component Layout	Depot Manual
g. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
h. Overall Interconnection	Figures FO-11,FO-12
i. Transceiver Assembly Schematic Diagrams	Depot Manual

5-58. OVERALL FRONT PANEL ASSEMBLY FUNCTION. The purpose of the Front Panel Assembly PWB is to provide a readout of 100 Watt Transceiver status signals, functions, frequency of operation, etc. For a discussion of all front panel functions, refer to chapter 4, table 4-1 and figure 4-1. As shown in the simplified functional diagram, figure 5-17, the Front Panel Assembly is essentially a serial-to-parallel shift register with input data loaded serially into the display decoders, and parallel outputs enabling the various display segments. Output data consists of 7 bits of binary data from the keypad decoder. The remaining circuits support the exchange of data and display devices.



5-17. Simplified Front Panel PWB

5-59. DETAILED FRONT PANEL ASSEMBLY CIRCUIT OPERATION. For the detailed technical discussion of the Front Panel Assembly, refer to the associated schematics. The front panel is the location for all transceiver analog controls, digital controls, operator interface jacks, switches, and the audio speaker. All the front panel elements are passive, except for the circuits for the digital keypad and LCD displays. Since the passive devices are readily understood from the schematic diagram, the technical discussion will be limited to the digital keypad and display circuit.

a. Front Panel Module Control Bus Interface Decoding. The FP-MCB interface for the Front Panel Assembly is entirely separate from the RF-MCB that services all other 100 Watt Transceiver assemblies. This is required due to the large amount of data activity required by the Front Panel Assembly. The operation of the FP-MCB is identical to the RF-MCB. However, only two of the possible sixteen addresses are used. The control signals for the Front Panel PWB are read into the assembly in a serial data stream. The MCB address strobe consists of two codes, one for the frequency display, and one for the meter display. The AD3-AD2-AD1-AD0 address for the frequency display is 0010 (2); for the meter display it is 0110 (6). Both Read and Write are decoded for the frequency display code, because the keypad readback uses this address, and only a Write function is decoded for the meter display. AD1 and AD0 are used as enables for 1-of-8 decoder U1, and AD3 and AD2 are used as decoder inputs along with the read/write strobe.

b. Meter Display MCB Write Cycle. When MCB data is intended for the meter display, the clock signal clocks serial bits of data into the Front Panel PWB U12-2 shift register port (via inverters U3B/U10D), continuing out of U12-9 and into Display PWB decoder U2. The meter display is associated with a 32 bit register and U12 is associated with an 8 bit register, therefore, for a meter display data write cycle, a total of 40 serial bits are loaded into the associated registers. Display PWB decoder U2 controls meter bar segments and related functions, while only one output of 8-bit register U12-4 is used to illuminate the front panel FAULT indicator. The U1-13 decoded strobe METER LOAD latches the data into the output storage registers of U12 and Display PWB decoder U2, completing a meter display MCB write cycle.

c. Frequency Display MCB Write Cycle. When MCB data is intended for the frequency display, the clock signal clocks serial data bits, via Front Panel PWB inverters U3B/U10D, into Display PWB decoder U3-34. This data is output at U3-35 into decoder U4-34, then into decoder U5-34, and finally into decoder U1-34. This path consists of 32 bits (U3) + 32 bits (U4) + 32 bits (U5) + 24 bits (U1) = 120 serial bits of data for a frequency display data write cycle. Notice that a portion of the meter display is actually serviced by the frequency display data stream. The Front Panel PWB U1-15 decoded strobe FREQUENCY LOAD latches the data into the corresponding output storage registers of the above mentioned decoders, completing a frequency display MCB write cycle.

d. Key Shift MCB Read Cycle. Data from the Front Panel PWB back to the control PWB is via an 8-bit parallel-to-serial converter, U4. During the microprocessor read function, the eight inputs to the parallel/serial register are read in serially to the Control PWB. The key shift strobe is generated from the Frequency Display address, plus the READ strobe at U1-14. The 7 bit inputs to U4 are from the front panel keypad (one U4 bit is not used). Therefore, the readback function of the Front Panel PWB is to route the keypad information back to the Control PWB. Five of the U4 parallel inputs are from the keypad decoder U2. The function of U2 is to decode three rows and five columns of the keypad into a binary output. The remaining two keypad columns (6 keys) are decoded by NAND gate U3, and flip- flop U9B.

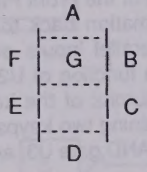
e. FP ATTENTION logic generation. When a key is pressed at the 100 Watt Transceiver front panel, the decoding of the selected key is latched into the internal U2 keypad decoder register. Simultaneuously, the U2-13 keypad decoder DATA AVAILABLE (DAV) port is set at logic high. After buffering by U7-B, the logic high clocks both U9A and U9B flip-flop. The clocking of U9A latches a logic high at the U9-5 Q output, which turns on transistor Q1. This places a ground on the FRONT PANEL ATTENTION line. The Control PWB receives this logic low as an interrupt signal and immediately strobes KEY SHIFT to get a readback of the new keypad status. The KEY SHIFT strobe enables the U4 shift register to send back the keypad information, and it clears flip-flop U9A for the next key activation.

f. Display Backlight Circuit. Lighting for the LCD displays is generated by U8. The input to U8 is +13.6 Vdc and the output is 115 Vac, 400 Hz, at 20 milliamperes. The output of U8 is divided into two

paths for the two display backlight inputs. U8 is a sealed assembly and not a serviceable item.

g. Backplane Oscillator. An LCD display operates by placing an oscillating voltage on the entire LCD backplane, and then placing the same oscillating voltage, 180 degrees out of phase, on the desired display segment to enable illumination. If the segment has an out-of-phase voltage applied, relative to the backplance oscillator, it illuminates; if the segment has an in-phase voltage applied, it does not illuminate. The backplane oscillator operates at a nominal 60 Hz, and is developed by U5- A/B. It is applied to the display BACKPLANE inputs, and to the display decoder LCD phase inputs. The actual switching of the backplane oscillator is internal to the decoder devices.

h. Display Device Encoding. The schematic diagram for the Display PWB identifies the decoder parallel outputs that illuminate the display segments. To clarify which codes are routed to the segments that form the alpha/numeric characters, refer to the code below:



The numbers in the frequency display are counted from left to right, i.e., the channel numbers are 9, 8, and frequency numbers are 7, 6, 5, 4, 3, 2, 1. For example, the segment 4A represents the frequency 10K digit, top segment.

5-60. TRANSCEIVER CONTROL PWB ASSEMBLY A1A12, 10085-9000. This manual portion describes the Transceiver Control PWB as an individual assembly. Section I of this chapter describes the function of the Transceiver Control PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. 8088 Microprocessor Figure 5-18

b. Simplified Microprocessor /Remote Interface Figure 5-19

c. Simplified Microprocessor READY/ENABLE Timing Figure 5-20

d. Simplified Select/Control Logic Figure 5-21

e. Simplified Memory Circuits Figure 5-22

f. Simplified A/D and D/A Conversion Circuits Figure 5-23

g. Simplified Interrupt Controller Circuits Figure 5-24

h. 8259 Programmable Interrupt Controller Figure 5-25

i. Simplified PPI Interface Circuits Figure 5-26

j. 8255A Programmable Peripheral Interface Figure 5-27

k. Schematic Diagram Depot Manual

l. Parts List Depot Manual

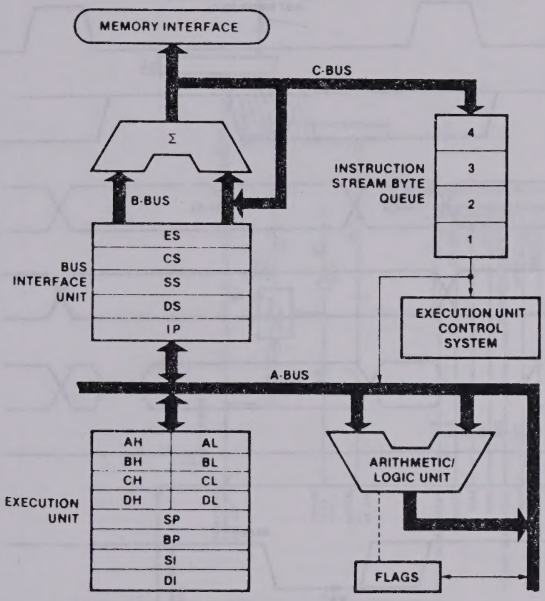
m. Component Layout Depot Manual

n. 100 Watt Transceiver Simplified Block Diagram Figure FO-1

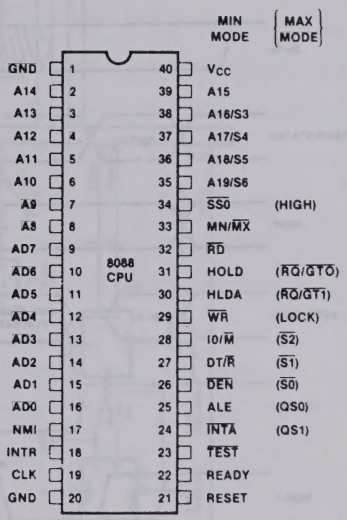
o. Overall Interconnection Figures FO-11, FO-12

p. Transceiver Assembly Schematic Diagrams Depot Manual

5-61. OVERALL TRANSCEIVER CONTROL PWB FUNCTION. The purpose of the Transceiver Control PWB is to provide control of the functions of the various elements within the transceiver, including front panel key selection, module control (via a Module Control Bus), BIT initiation and readout, fault, meter, and status indications; and the remote control data interface. The key element in the control function is the 8088 microprocessor. It is assumed the user has a working knowledge of microprocessor theory, the discussion of which is beyond the scope of this manual. Discussion of the software is also beyond the scope of this manual. Therefore, the theory of operation covers only the Control Board hardware, which is divided into six segments. Use the simplified drawings supplied with the description of each segment when general knowledge of the



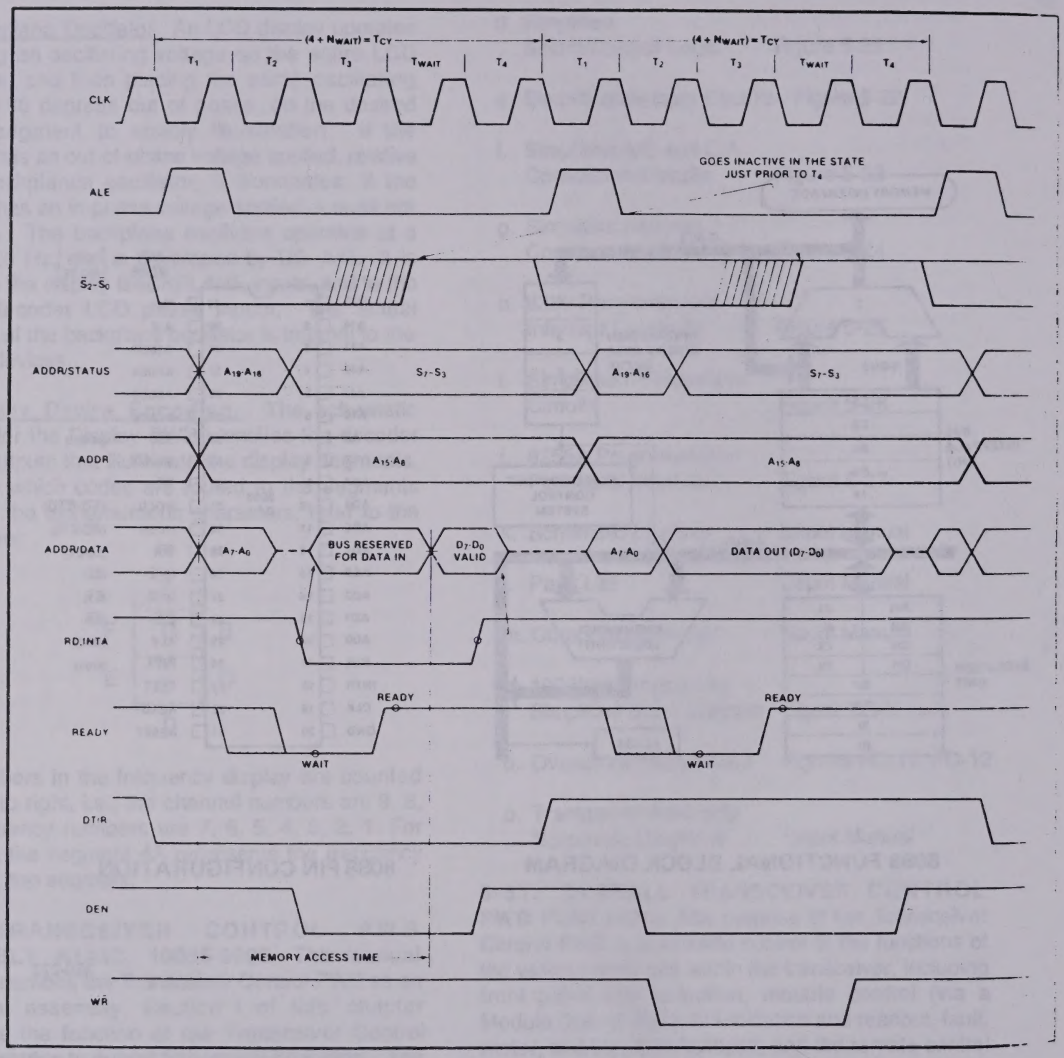
8088 FUNCTIONAL BLOCK DIAGRAM



8088 PIN CONFIGURATION

350-023

Figure 5-18. (Sheet 1 of 2) Summary of 8088 Microprocessor Specification



8088 BASIC SYSTEM TIMING

350-024

Figure 5-18. (Sheet 2 of 2) Summary of 8088 Microprocessor Specification

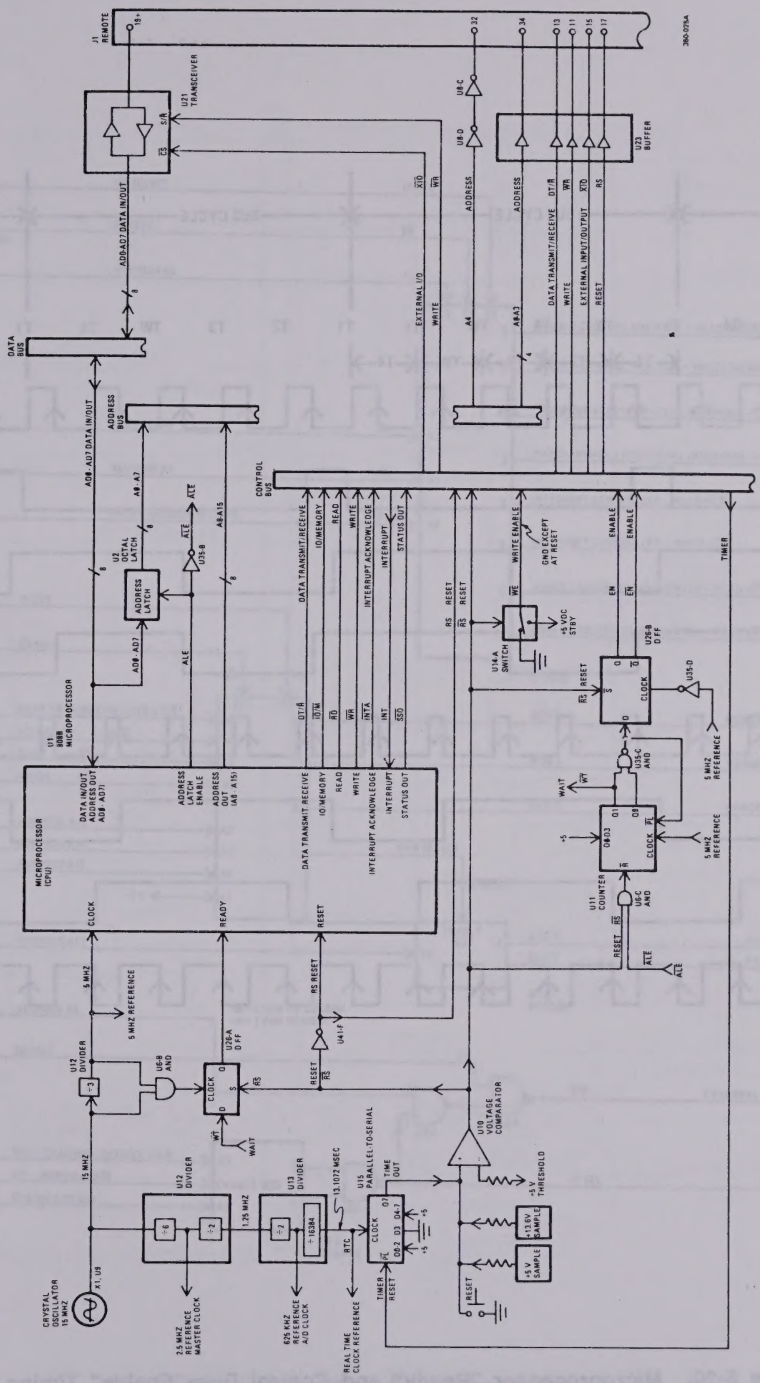


Figure 5-19. Simplified Microprocessor/Remote Interface

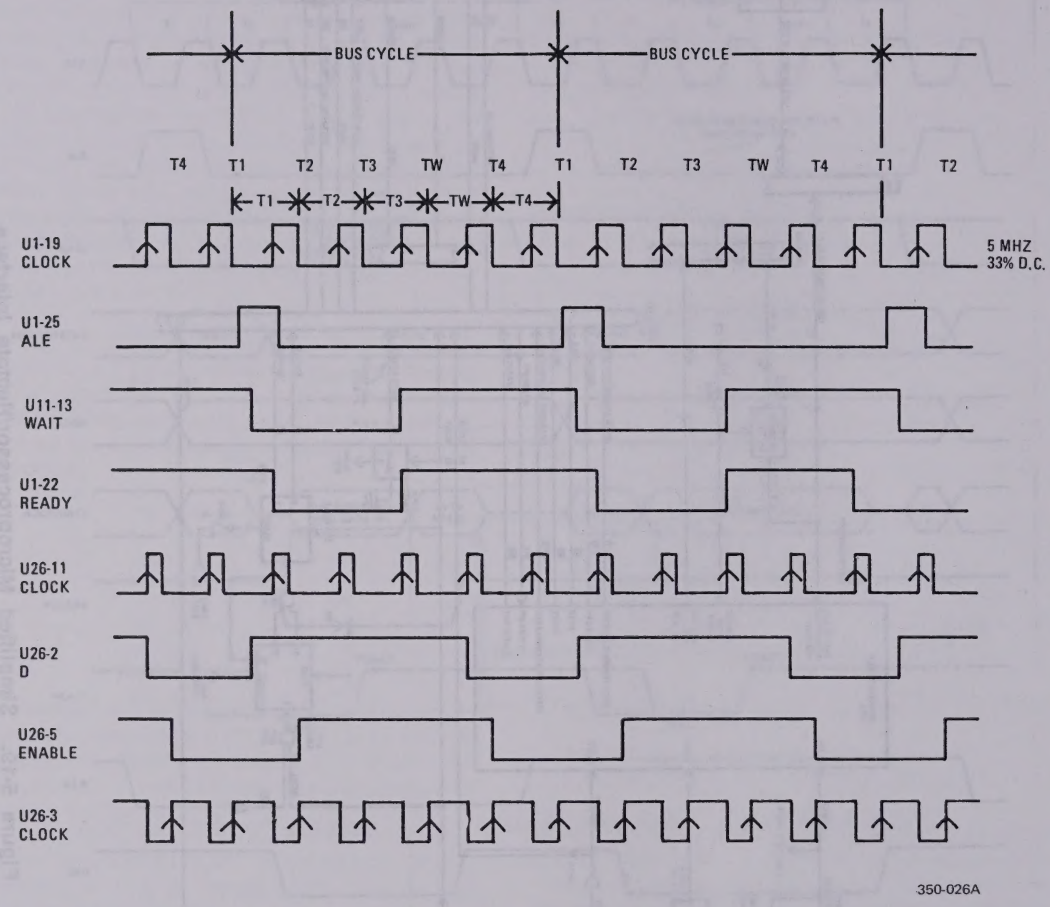


Figure 5-20. Microprocessor "Ready" and Control Bus "Enable" Timing Chart

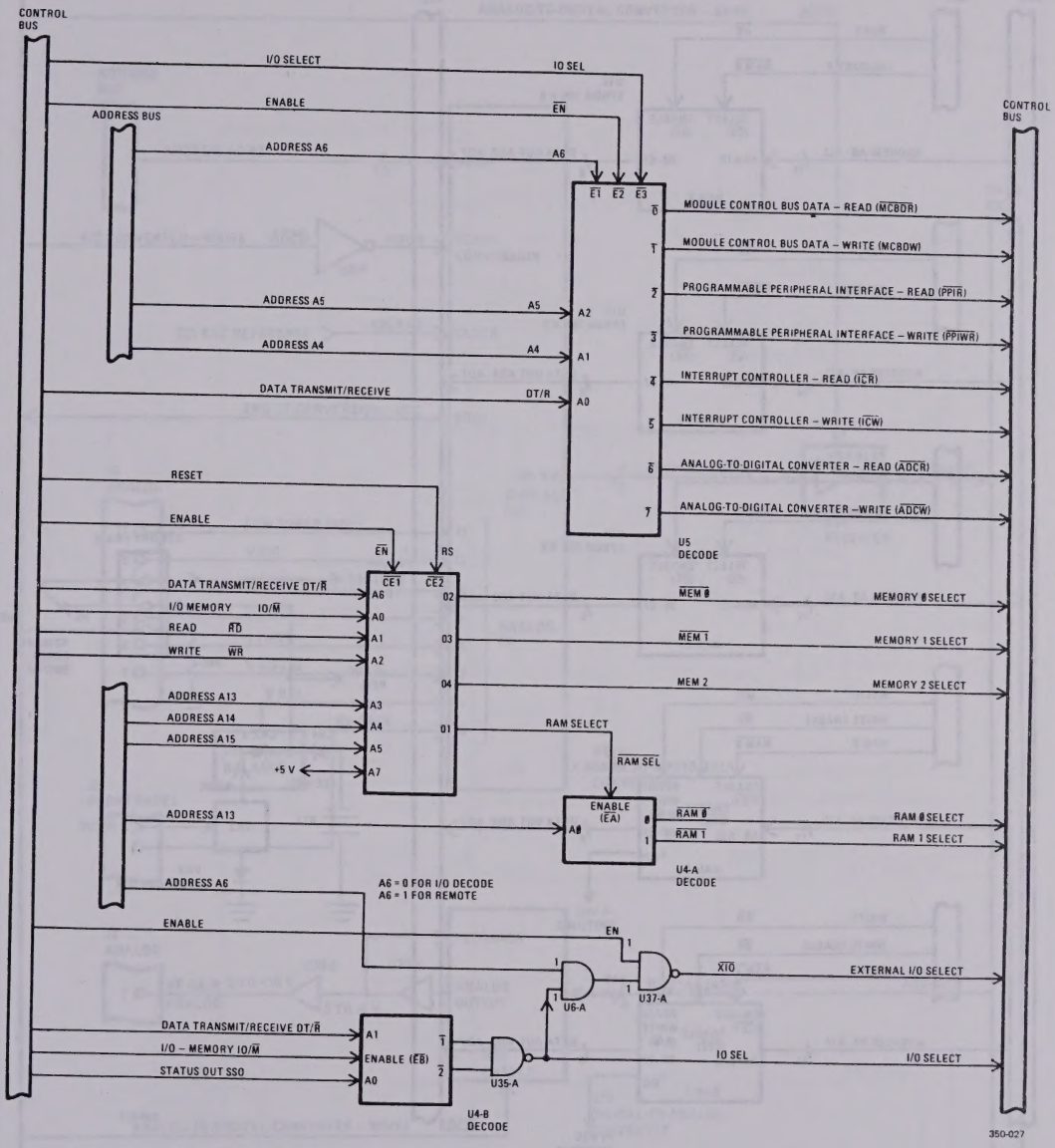


Figure 5-21. Simplified Select/Control Logic

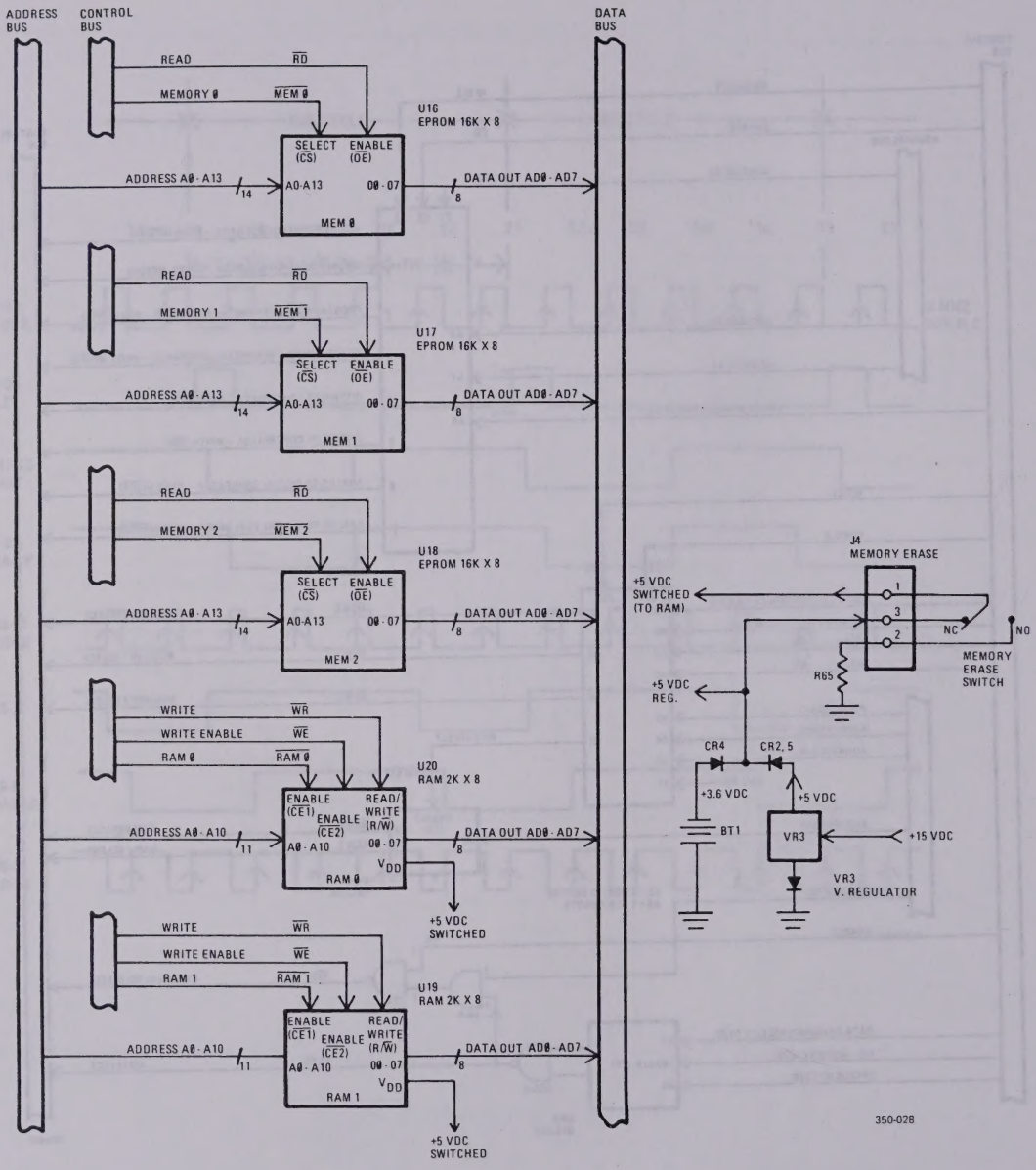
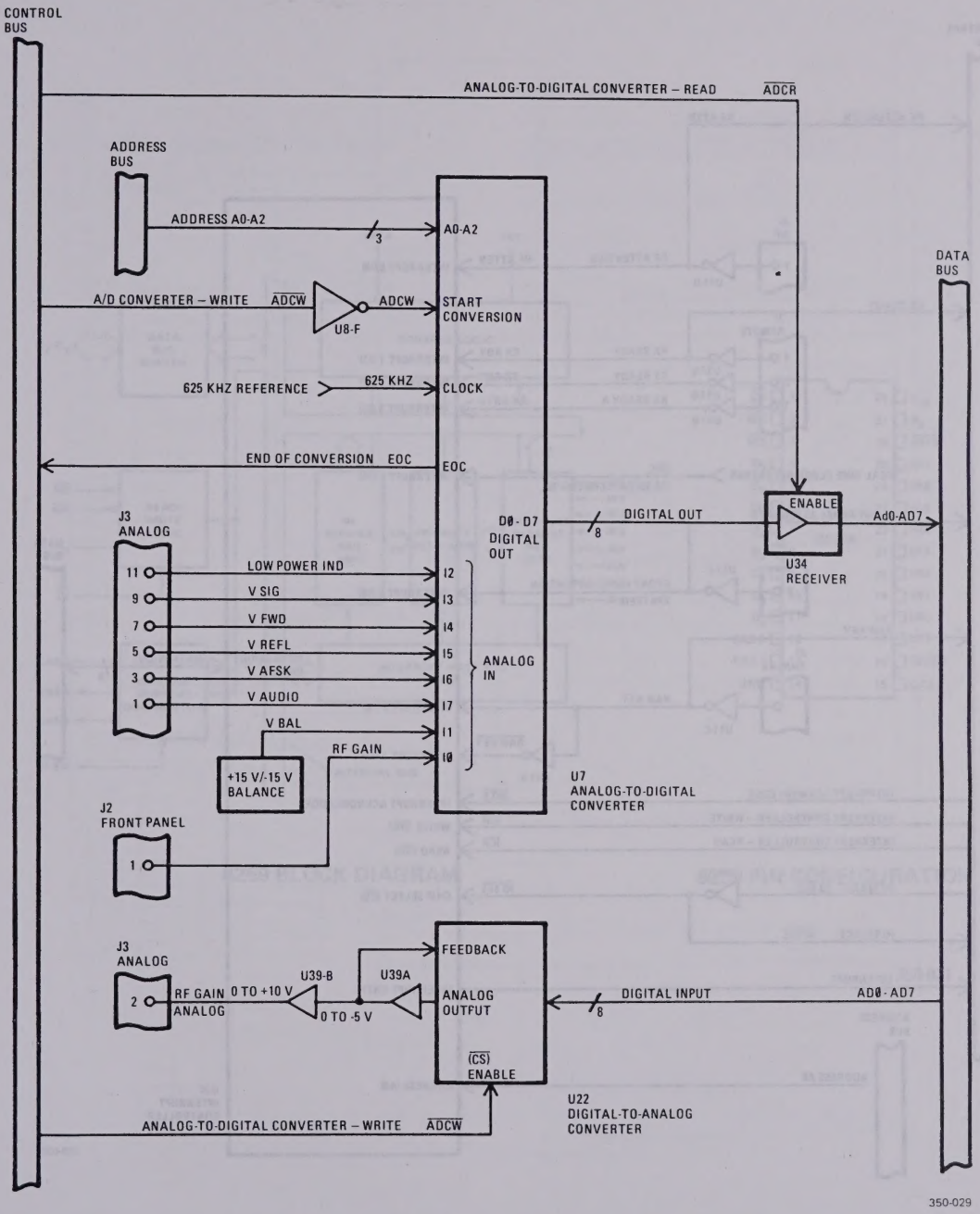


Figure 5-22. Simplified Memory Circuits



350-029

Figure 5-23. Simplified A/D - D/A Conversion Circuits

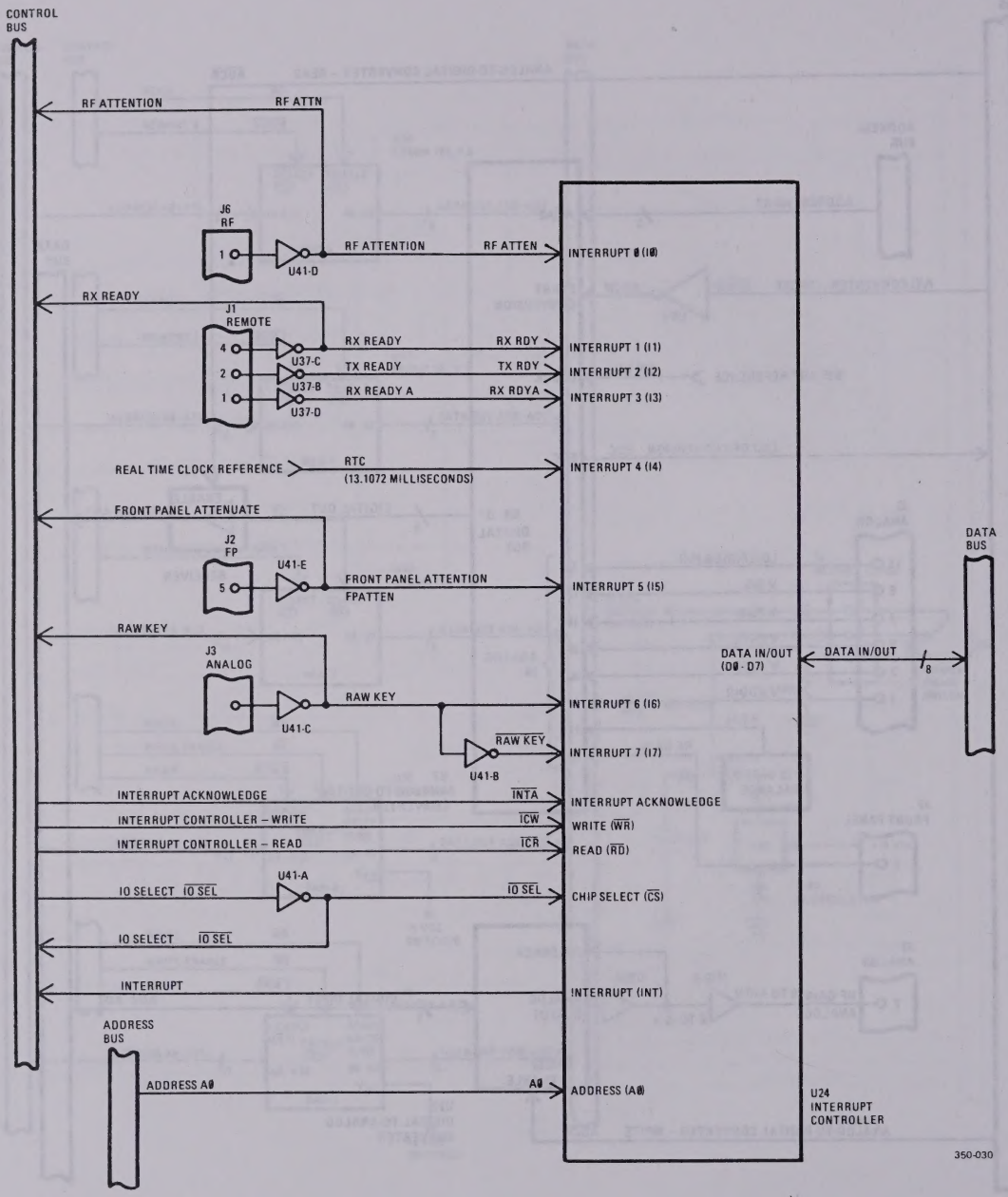
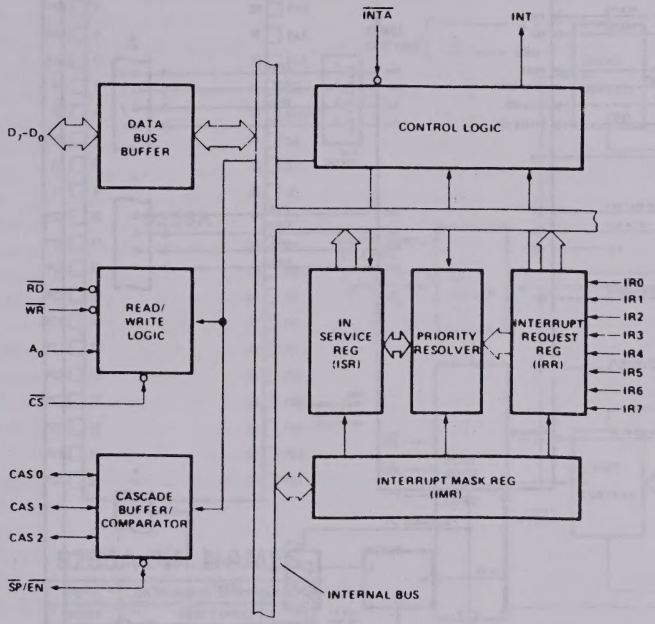
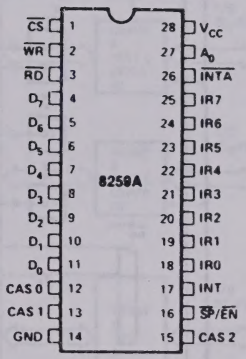


Figure 5-24. Simplified Interrupt Controller Circuits



8259 BLOCK DIAGRAM



8259 PIN CONFIGURATION

350-031

Figure 5-25. Summary of 8259 Programmable Interrupt Controller

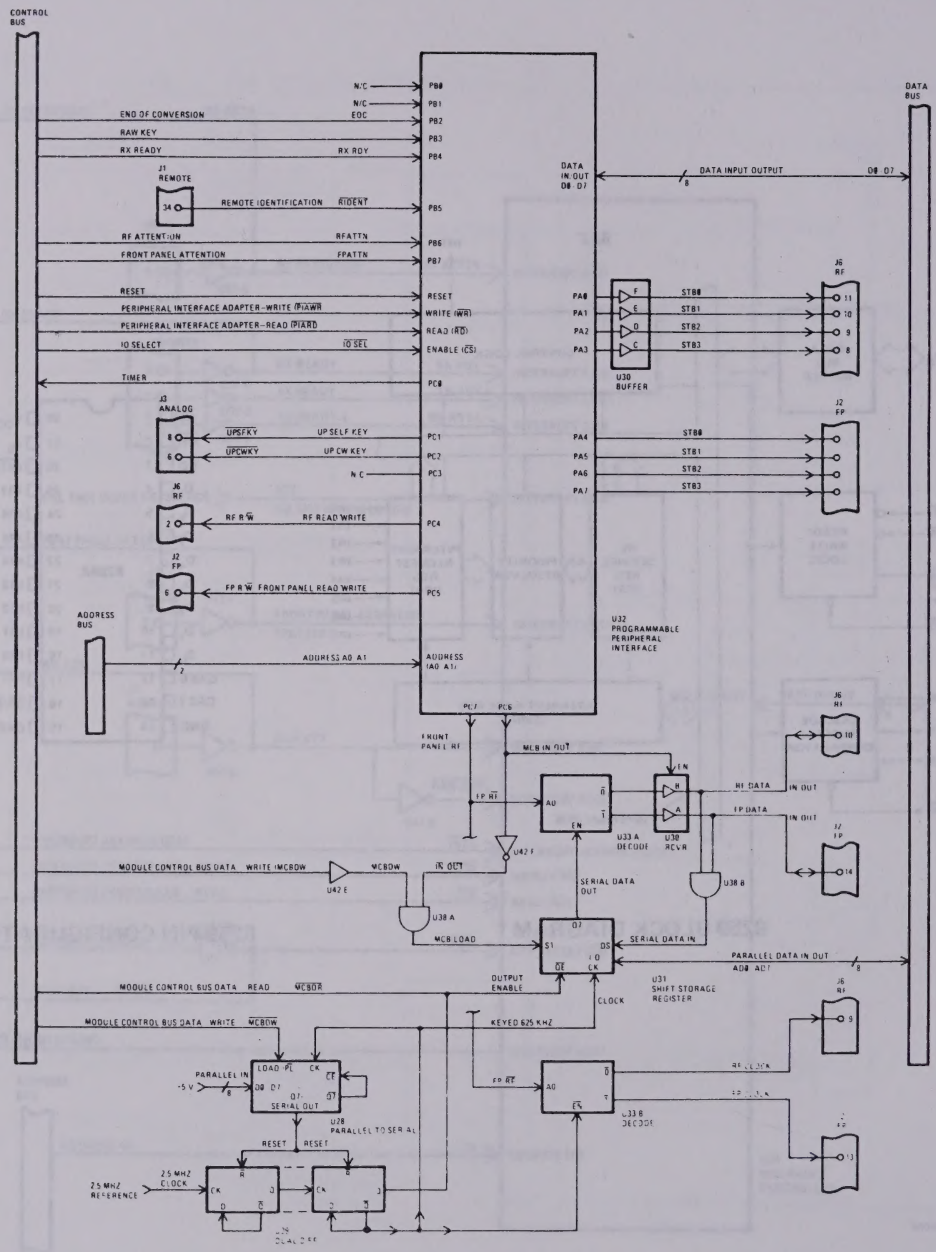
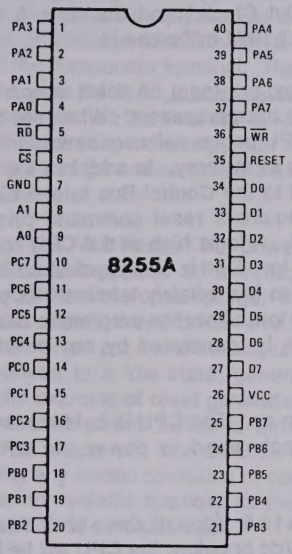
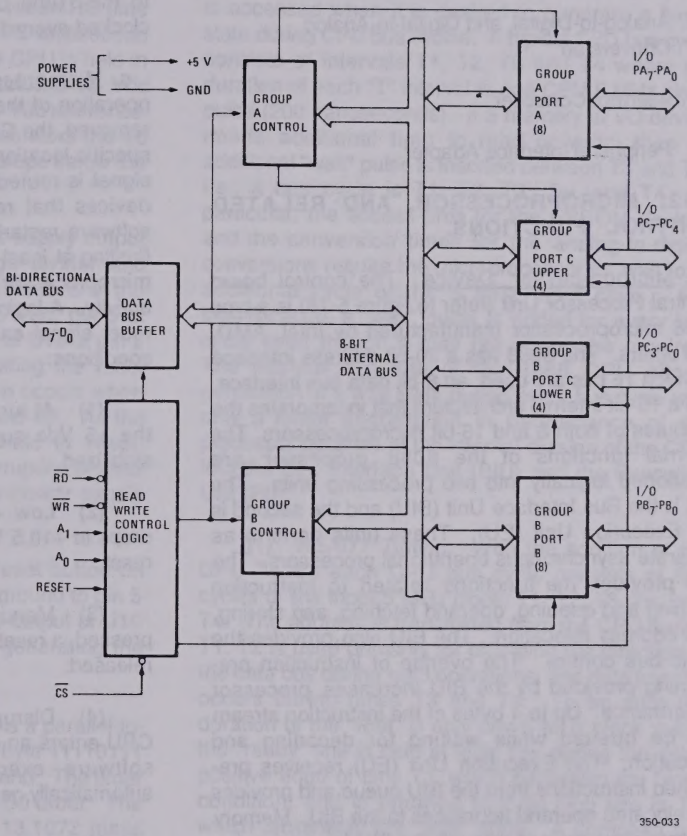


Figure 5-26. Simplified Programmable Peripheral Interface Circuits

8255A PIN CONFIGURATION



8255A BLOCK DIAGRAM



8255A PIN NAMES

D_7-D_0	DATA BUS (BI DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{cc}	+5 VOLTS
GND	0 VOLTS

Figure 5-27. Summary of 8255A Programmable Peripheral Interface Specifications

control board is sufficient, and the schematic diagram when detailed analysis is required. The six segments that will be discussed are:

a. Microprocessor

b. Select/Control Logic

c. Memory

d. Analog-to-Digital, and Digital-to-Analog Conversion

e. Interrupt Controller

f. Peripheral Interface Adapter

5-62. MICROPROCESSOR, AND RELATED CONTROL FUNCTIONS.

a. Microprocessor Device. The control board Central Processor Unit (refer to figure 5-18) is a type 8088 microprocessor manufactured by Intel, AMD, and others. The 8088 has a 20-bit address interface of which 16 bits are used, an 8-bit data bus interface, and a 16-bit internal architecture that incorporates the attributes of both 8 and 16-bit microprocessors. The internal functions of the 8088 processor are partitioned logically into two processing units. The first is the Bus Interface Unit (BIU) and the second is the Execution Unit (EU). These units perform as separate asynchronous operational processors. The BIU provides the functions related to instruction fetching and queuing, operand fetching, and storing, and address relocation. The BIU also provides the basic bus control. The overlap of instruction pre-fetching provided by the BIU increases processor performance. Up to 4 bytes of the instruction stream can be queued while waiting for decoding and execution. The Execution Unit (EU) receives pre-fetched instructions from the BIU queue and provides un-relocated operand addresses to the BIU. Memory operands are passed through the BIU for processing by the EU, which passes results to the BIU for storage.

b. Microprocessor Clock. The microprocessor clock input is 5 MHz and provides the basic timing for the processor. (Refer to figure 5-19.) It is asymmetric with a 33% duty cycle which optimizes internal timing. The CPU 5 MHz clock is derived from a 15 MHz crystal oscillator output which is divided by 3 with U12. U12 has two other outputs: a divide-by-six output for the 2.5 MHz "Master Clock", and a divide-by-12 1.25 MHz reference output that is divided further by U13. The 1.25 MHz reference is applied to 14 stage ripple counter U13 where a progressive number of stages divide the input by 2. The ADC CLOCK output at U13-Q1 is 625 KHz, and is used as the clock for the analog-to-digital converter. The U13-Q14 output divides the 1.25 MHz input by 16,384 which yields an output pulse every 13.1072 milliseconds and is the "Time Out Clock". The "Real Time Clock" is strapped to the "Time Out Clock," and therefore it is also clocked every 13.1072 milliseconds.

c. Microprocessor Reset. A reset suspends the operation of the microprocessor. When the reset is removed, the CPU begins software execution from a specific location in memory. In addition, the "reset" signal is routed to the Control Bus to service other devices that require a reset command prior to a software restart. A logic high at the CPU reset pin (lasting at least four 5 MHz clock cycles) causes the microprocessor to immediately terminate its present activity. A logic low allows the program to restart. A reset signal can be generated by any of following conditions:

(1) At turn on: The CPU is held in reset until the +5 Vdc supply used to power the CPU has stabilized.

(2) Low +13.6 Vdc: If the +13.6 Vdc level drops to +10.5 Vdc or below, the CPU will be held in reset.

(3) Manual reset: If the manual reset button is pressed, a reset signal is generated until the button is released.

(4) Disruption of software execution: If the CPU enters an operating mode that prevents normal software execution, a timer will time-out and automatically generate a reset signal.

d. Microprocessor Reset Command Generation. The microprocessor reset is generated from one of the following circuits:

(1) Comparator device. The reset signal is generated by quad voltage comparator U10. U10 has open collector outputs, i.e., if a high output state is tied to a low potential, the combined output is forced to the low potential. When the (+) terminal of the voltage comparator is at a lower potential than the (-) terminal, the output of the comparator will be at low potential. The reference voltage (Vref) for the U10

comparator is actually the supply voltage for the RAM memory devices. The generation of this voltage is discussed in the CPU memory.

(2) Turn-on and +5 Vdc Reset. A voltage comparison is made between a voltage reference and the +5 Vdc power supply. The voltage reference appears at turn-on on U10 pin 8 before the +5 Vdc supply voltage begins to appear on U10 pin 9. In addition, the +5 Vdc supply sample is via an RC time constant (R14/C4) which inserts a 75 millisecond delay at the comparator terminal. The CPU is held in reset, i.e., pin 14 is at low level, until the +5 Vdc supply has reached the level of the +5 Vdc reference. After initial turn-on, the comparator monitors the +5 Vdc supply and generates a reset if it drops below the threshold level.

(3) 13.6 Vdc Reset. The power supply output of +13.6 Vdc is applied to a voltage divider and compared with a reference voltage. If the level of the +13.6 Vdc supply drops below +10.5 Vdc, pin 5 of U10 will be below pin 4 and the output of U10 at pin 2 will be driven to a low state, generating the reset signal. An example of reset generation occurs when the transceiver power switch is turned off. As the +13.6 Vdc drops off, the CPU is held in reset, preventing any erratic operation or corruption of data stored in non-volatile memory as the power supply voltages settle to zero potential.

(4) Manual Reset. A manual reset button on the board can be selected, applying a ground to pin 5 of U10, which will be below pin 4. The output of U10 at pin 2 will be driven to a low state, generating the reset signal.

(5) Time-out Reset. Timer U15 is a parallel-to-serial IC that loads a parallel 8-bit data byte 11110111 (D7-D0) with every input "timer" command. The timer then serially clocks the data out in D7-D0 order. The input clock signal is strapped to the 13.1072 msec Real Time Clock (RTC). If the timer is not re-loaded with an input "Timer" control pulse, at the forth RTC pulse U15 will serially clock out the logic "0" on its Q7 output. The logic "0" places voltage comparator U10 pin 7 below the reference voltage at U10 pin 6, forcing U10 pin 1 to a low condition. This in turn forces pin 5 of U10 below the reference voltage at pin 4, and U10 pin 2 switches to a low condition, i.e., reset. During normal operation, the timer is re-loaded before a logic "0" is clocked out. The "Timer" control pulse is generated through software processing of a Real Time Clock interrupt. If the CPU enters a non-standard operating condition in which the software program is not being executed, the CPU will be unable to service the Real Time Clock interrupt, the U15 timer will not be re-loaded, and a reset signal will be generated.

e. Microprocessor Ready. For the discussion of the "Ready" and "Enable" logic refer to timing diagram, figure 5-20. The microprocessor ready line is accessed when it is desired to generate a "wait" state during CPU bus cycles. A typical CPU bus cycle consists of intervals T1, T2, T3 and T4 where the duration of each "T" interval is one CPU 5 MHz clock pulse (200 nanoseconds). If a memory or I/O device needs additional time to read or write, then an additional "wait" pulse is inserted between T3 and T4, i.e., a bus cycle is T1, T2, T3, Tw, and T4. In particular, the access time for the EPROM devices and the conversion times for the analog-to-digital conversions require the microprocessor to "wait" one additional cycle of the 5 MHz input clock. For simplification, a "wait" pulse is added for every bus cycle even though it may not always be required. The internal structure of the 8088 CPU allows generation of a wait state during every bus cycle with only a minor degradation in performance of the processor because of the internal division of the CPU into the Bus Interface Unit (BIU) and the Execution Unit (EU).

(1) READY Timing. With the addition of the CPU "wait", each CPU bus cycle consists of five cycles of the input 5 MHz clock; T1, T2, T3, Tw, and T4. The address is transmitted from the CPU during T1; T2 is used primarily for changing the direction of the data bus during read operations; and data transfer occurs during times T3 and T4. To be sure the duration of the "wait" is only one 5 MHz clock pulse, the "ready" line is held at logic low during the rising positive edge of time T3, which generates the "wait" condition, and is returned to logic high late in T3, which terminates the "wait" state. A complete bus cycle is not always T1, T2, T3, Tw, T4. The CPU may insert Ti (Idle) 5 MHz clock cycles for internal housekeeping as required, i.e., T1, T2, T3, Tw, T4, Ti. To generate the proper timing for "Ready", two signals are used. First is the 5 MHz CPU clock input; second is the Address Latch Enable (ALE) signal generated during T1. It will be assumed that no "reset" command occurs.

(2) Reset by Counter U11. Counter U11 is "master reset" to zero by ALE during time T1, i.e., all the U11-Q outputs are forced to a logic low. In

particular Q1/Q0 are 0,0. The Q1 output is the "wait" line where "wait" is logic 0 and Tw is enabled via U26-A. ALE releases the master reset condition slightly after the rising positive edge of T2. The next 5 MHz clock pulse, T3, increments the U11 counter Q1/Q0 outputs to 0,1 as the counter begins to count up in BCD. The next 5 MHz clock pulse, Tw, increments the U11 counter outputs to 1,0 (Q1/Q0). When Q1 is at logic 1, the "wait" command is removed.

(3) Wait by Flip-flop U26A. The U11-Q1 output ("wait") of the counter is further controlled by flip-flop U26A where it is used as the flip-flop "D" input. The clock input for U26-A is 5 MHz ANDed with 15 MHz, resulting in a 5 MHz signal with a narrower duty cycle and with a rising positive edge occurring after the 5 MHz CPU clock rising positive edge. The logic status at U26-A "D" input ("wait") is clocked through to the U26-A "Q" output ("ready") with the narrower clock pulse. This results in the "ready" line going to logic 0 during T2, and remaining low during the rising edge of T3, which advises the CPU to inject a "wait" pulse. The "ready" line is returned to logic 1 at the end of T3, which assures the "wait" will last only for the duration of one 5 MHz cycle.

f. Microprocessor Address Latch Enable. The lower 8 bits of the 16 bit CPU address bus are time multiplexed with the 8 bit data bus to reduce the pin count of the CPU device. This means the lower bits AD0-AD7 are used for two functions during CPU cycling. At the start of a bus cycle (during T1), the address appears on pins AD0-AD7 and is latched into U2 when the "Address Latch Enable" (ALE) output is toggled from high to low. After ALE (during T2), AD0-AD7 becomes a two-way data bus, with U2 holding the address for the remainder of the bus cycle. The address byte A8-A15 is present during the entire bus cycle and does not require an address latch. .Bits A16-A19 are not used.

5-63. ENABLES FOR CONTROL BUS ACTIVITY. The "enable" signal is used to enable CPU bus activity for memory and I/O activities only during bus cycle times T2, T3 and Tw, as counted by counter U11. Bus access is further restricted by use of the 8088 control outputs. Counter U11, which counts CPU clock pulses and is reset by ALE, has outputs Q1/Q0 which are NANDed to provide the "D" input to the U26-B flip-flop. Refer to the "Counter U11" discussion above for generation of the CPU "ready" signal up to the point of 5 MHz clock pulse Tw. The next 5 MHz clock (T4) advances counter U11 to 1,1 (Q1/Q0). NAND gate U35 now has both inputs at logic 1 and the output of U35 goes to logic 0. The logic 0 output of NAND gate U35 enables the "parallel load" for counter U11. Since all the counter inputs (D0-D3) are tied to +5 Vdc, the parallel load forces all U11 Q outputs to logic 1. Although Q1/Q0 were already at logic 1, the forcing has disabled the counter (the counter can't advance until the "parallel load" is removed and the load cannot be removed until the counter is advanced). This condition will not change until a "master reset" occurs, as discussed for the CPU "ready" condition. Then the cycle repeats.

a. Generation of Control Bus ENABLE. The logic 0 at the output of NAND U35 is also applied to the "D" input of U26-B. The clock for U26-B is the CPU 5 MHz clock passed through an inverter. The inverter advances the rising positive edge of the clock pulse relative to the U11 counter clock pulse. The rising positive edge of the U26-B clock pulse loads the U26-B status at the "D" input to the "Q" output ("enable"). The timing of this action generates "enable" during time T2 and "disable" at the start of pulse T4. The complementary output of U26-B, Q-not, is also used for circuits that require a logic low for "enable". Both states of the "enable" signal are applied to the "control bus" and will be referenced in other circuit descriptions.

b. Generation of WRITE ENABLE. The "write enable" is a control signal used to inhibit the RAM memory "write" function whenever the CPU is in "reset". (See the previous discussion for generation of the CPU "reset" command.) When the "write enable" is at logic high, the RAM write function is disabled to prevent the writing of incorrect data into the RAM, or the overwriting of desired RAM data. When "write enable" is at logic low, the RAM's "write" function is enabled. Bilateral switch U14 connects "write enable" to ground so long as the CPU reset line is high (no reset). If the CPU reset line goes low (reset), then switch U14 opens and "write enable" is connected to Vstby (Voltage Standby). Vstby is the voltage line for the RAM power source. When the transceiver is powered, Vstby is the output from +5 Vdc voltage regulator VR3; when the transceiver is unpowered, Vstby is the output from the RAM memory +3.6 Vdc lithium battery.

5-64. REMOTE CONTROL INTERFACE. Connector J1 is used to interface with the remote control assembly, which is treated by the CPU as an external input/output device (XIO). All bus signals to and from J1 are buffered to isolate the remote control board from the control board.

a. Remote Control Data Bus. The two-way data bus AD0-AD7 is buffered by transceiver U21. U21 has control ports "Chip Select" and "Send/Receive". The U21 "Chip Select" port is enabled by Control Bus input "External I/O Select", which is discussed in a separate paragraph.

b. Remote Control Send/Receive Control. The "Send/Receive" logic for transceiver U21 is the "Write" command from the CPU. When "Write" is logic low, U21 is in the "Receive" mode, i.e., data is flowing from the CPU to the Remote Assembly. When "Write" is logic high, U21 is in the "Send" mode, i.e., data is flowing from the Remote Assembly to the CPU.

c. Remote Control Address and Control Signals. All remote control address and control signal lines are buffered by line driver U23 except for address A4, which is buffered by inverters in U8. The following address and control signals are buffered and sent to the Remote Assembly:

(1) Address A0, A1, A2, A3 and A4

(2) "Data Transmit/Receive" (DT/R)

(3) "Write" (WR)

(4) "External I/O" (XIO)

(5) "Reset" (RESET)

d. Remote Control Ready Inputs to Control Board. The ready inputs from the Remote Control to the Control Board are buffered and inverted by NAND gate U37. The three ready inputs to the control board are:

(1) "TX Ready" (TxRDY)

(2) "RX Ready" (RxRDY)

(3) "RX Ready-Auxiliary" (RxRDY AUX)

e. Remote Identity Input. When a Remote Assembly is installed in a transceiver, a Remote Assembly input connector pin is grounded to provide a status line to the CPU. The CPU monitors the "Remote Indicator" (RIND), line, which is logic 0 when the remote board is installed and logic 1 when the remote board is not installed. If the Remote Assembly is not installed, the CPU will not respond to commands to go into the remote mode of operation. A complete discussion of the Remote Assembly, including the CPU interface, will be found in the manual for the Remote Control Unit (see Table 1-4).

5-65. INPUT/OUTPUT DEVICE SELECT /CONTROL LOGIC GENERATION. The select and control functions are generated with PROM (256x4) U3, Dual 2-to-4 Decoder U4, and 3-to-8 Decoder U5. Inputs to these devices are from the CPU control and address lines. The outputs are directed to memory and I/O devices, including the "read" and "write" enables for each.

a. Memory Decoder Prom. Refer to figure 5-21. The U3 PROM outputs are select lines generated from the pattern of the input status signals. The PROM bit map is provided in table 5-4. The PROM inputs are all from the CPU; the enable signals are "reset" and "enable", which were previously discussed. The software program controls the pattern of the CPU output lines, which is decoded by U3. The "RAM Select" output is decoded further by U4-A since there are two RAM devices. After decoding, only one of the following outputs is selected:

(1) "RAM Select" (RAM's U19 and U20)

(2) "Memory 0 Select" (EPROM U16)

(3) "Memory 1 Select" (EPROM U17)

(4) "Memory 2 Select" (EPROM U18)

b. Memory Decoding. The "RAM Select" output from PROM U3 is used as the Memory Decoder U4A enable. Therefore, U4A will have an output only when "RAM Select" is present. Address bit A13 provides the logic input to the decoder input A0, selecting output "RAM 0" if A13 is logic 0, or output "RAM 1" if A13 is logic 1. These status signals are then routed to the corresponding RAM device.

c. I/O and External I/O Decoding. The output of the U4B decoder is the command line "I/O SELECT". "I/O Select" is generated by decoder U4B and NAND gate U35 to prevent I/O devices from being selected except during I/O read or write portions of the bus cycles. The CPU can be in one of eight states during a bus cycle, all of which can be decoded as shown in table 5-4.

Table 5-4.
BIT MAP FOR MEMORY DECODE PROM U3

Code is listed in hexadecimal format:

Binary	Hexadecimal (Hex)
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001	9
1010	A
1011	B
1100	C
1101	D
1110	E
1111	F

The bit map Hex is decoded for the address and data information. An example is shown below:

AD	DA		ADDRESS								DATA			
			A7	A6	A5	A4	A3	A2	A1	A0	O4	O3	O2	O1
2C	D	===>	0	0	1	0	1	1	0	0	1	1	0	1
			[		2		] [		C	]	[		D	]

PROM format is 256x4, where an 8-bit input address (A0-A7) identifies one of the 256 4-bit outputs (O1-O4).

AD	DA	AD	DA	AD	DA	AD	DA	AD	DA	AD	DA	AD	DA	AD	DA
00	F	10	F	20	F	30	F	40	F	50	F	60	F	70	F
01	F	11	F	21	F	31	F	41	F	51	F	61	F	71	F
02	F	12	F	22	F	32	F	42	E	52	F	62	F	72	B
03	F	13	F	23	F	33	F	43	F	53	F	63	F	73	F
04	E	14	F	24	F	34	B	44	E	54	F	64	F	74	B
05	F	15	F	25	F	35	F	45	F	55	F	65	F	75	F
06	F	16	F	26	F	36	F	46	F	56	F	66	F	76	F
07	F	17	F	27	F	37	F	47	F	57	F	67	F	77	F
08	F	18	F	28	F	38	F	48	F	58	F	68	F	78	F
09	F	19	F	29	F	39	F	49	F	59	F	69	F	79	F
0A	F	1A	F	2A	F	3A	F	4A	E	5A	F	6A	D	7A	7
0B	F	1B	F	2B	F	3B	F	4B	F	5B	F	6B	F	7B	F
0C	E	1C	F	2C	D	3C	7	4C	E	5C	F	6C	D	7C	7
0D	F	1D	F	2D	F	3D	F	4D	F	5D	F	6D	F	7D	F
0E	F	1E	F	2E	F	3E	F	4E	F	5E	F	6E	F	7E	F
0F	F	1F	F	2F	F	3F	F	4F	F	5F	F	6F	F	7F	F
80	F	90	F	A0	F	B0	F	C0	F	D0	F	E0	F	F0	F
81	F	91	F	A1	F	B1	F	C1	F	D1	F	E1	F	F1	F
82	F	92	F	A2	F	B2	F	C2	E	D2	D	E2	B	F2	7
83	F	93	F	A3	F	B3	F	C3	F	D3	F	E3	F	F3	F
84	E	94	D	A4	B	B4	7	C4	E	D4	D	E4	B	F4	7
85	F	95	F	A5	F	B5	F	C5	F	D5	F	E5	F	F5	F
86	F	96	F	A6	F	B6	F	C6	F	D6	F	E6	F	F6	F
87	F	97	F	A7	F	B7	F	C7	F	D7	F	E7	F	F7	F
88	F	98	F	A8	F	B8	F	C8	F	D8	F	E8	F	F8	F
89	F	99	F	A9	F	B9	F	C9	F	D9	F	E9	F	F9	F
8A	F	9A	F	AA	F	BA	F	CA	E	DA	D	EA	B	FA	7
8B	F	9B	F	AB	F	BB	F	CB	F	DB	F	EB	F	FB	F
8C	E	9C	D	AC	B	BC	7	CC	E	DC	D	EC	B	FC	7
8D	F	9D	F	AD	F	BD	F	CD	F	DD	F	ED	F	FD	F
8E	F	9E	F	AE	F	BE	F	CE	F	DE	F	EE	F	FE	F
8F	F	9F	F	AF	F	BF	F	CF	F	DF	F	EF	F	FF	F

	Logic from CPU			Bus Cycle	"I/OSelect"
	IO/M	DT/R	SSO		
	1	0	0	Code Access	Disable
M	1	0	1	Read Memory	Disable
= 1	1	1	0	Write Memory	Disable
	1	1	1	Passive	Disable
	0	0	0	Interrupt Acknowledge	Disable
I/O	0	0	1	Read I/O Port	Enable
= 0	0	1	0	Write I/O Port	Enable
	0	1	1	Halt	Disable

Note

Logic is referenced to U4-B inputs.

d. I/O Select Timing. Referring to the table above, the logic required for U4-B and U35 to generate an "I/O Select" command is present only during the "Read I/O Port" and "Write I/O Port" bus cycle. The U4-B decoder outputs combined with NAND U35 yield the desired "I/O Select" command. "External I/O Select" is generated when all the conditions required for "I/O Select" are met and, in addition, address A6 is a logic 1 and "Enable" is a logic 1 at the inputs of AND gate U6A. Address A6 is set to logic 1 for remote I/O and logic 0 for local (on board) I/O. "External I/O Select" is used only in conjunction with the remote control feature as a "chip select" for data transceiver U21.

e. Control Board I/O Devices. Four local I/O devices communicate with the CPU (remote control is a remote I/O device and is not included). The U5 decoder generates the required select and control logic for each of these four I/O devices:

(1)	Module Control Bus Data	Read and Write
(2)	Programmable Peripheral Interface	Read and Write
(3)	Interrupt Controller	Read and Write
(4)	Analog/Digital Converter	Read and Write

f. Control Board I/O Device Timing. The U5 enable inputs "I/O Select" and "Enable" allow I/O activity only during the correct portion of the CPU bus cycle. The address bit A6 is coded to be a logic low for local I/O (logic 1 for remote I/O) and is the last of the three U5 enables. The input lines that are decoded include two CPU address bits, A4 and A5, and the CPU output logic "Data Transmit/Receive". The selected output of U5 is a logic low, i.e., the selected line is 0 and the remaining seven lines are 1. The inputs to gates U6 and U37 used to generate "External I/O Select" are identical to the U5 decoder enable inputs. The only difference is the logic of address A6, which is low for local I/O and high for remote I/O. The address bits are decoded for selection of the I/O device and the "Data Transmit/Receive" logic determines if the selected I/O device is to read or write as shown below:

Address A5	Address A4	I/O Device Selected
0	0	Module Control Bus
0	1	Peripheral Interface Adapter
1	0	Interrupt Controller
1	1	A/D and D/A Converters

"Data Transmit/Receive"
= 1 for Transmit (write to I/O))
= 0 for Receive (read from I/O)

5-66. MEMORY DEVICES. A total of five memory devices operate in conjunction with the CPU. Three EPROM (Eraseable Programmable Read-Only Memory) devices store the software routines for the CPU, and two RAM (Random Access Memory) devices are used for data storage for CPU and radio operation. The CPU does not discern separate memory devices, rather, it views memory as a single entity. It is through the software programming of the CPU that the correct memory device is selected, written to, or read from, through select logic and addressing. The outputs of the memory devices are connected in parallel and form a portion of the data bus.

a. EPROM Devices. Refer to figure 5-22. EPROM devices U16, U17 and U18 are memory elements used to store the software routines and instructions for operation of the 8088 Central Proccesor Unit (CPU). There is no "write" function for the EPROM's. Information is read from the devices only. Programming of the EPROM's is a factory function. Although the devices are eraseable by placing them in ultraviolet light, actual erasure is reserved for factory operations to allow upgrade and flexibility in any future program changes. The user should never attempt to erase an EPROM. Two types of pin compatible EPROM's may be installed in the transceiver; EPROM 2764 with 8K x 8 format, or EPROM 27128 with 16K x 8 format. With EPROM 27128, the address A0-A13 (14 bits) can access 16,384 (16K) 8-bit bytes. With EPROM 2764, the address A0-A12 (13 bits) can access 8,192 (8K) 8-bit bytes. All standard transceivers have the EPROM 27128 with 16K x 8 format installed.

b. EPROM Enables. Each EPROM has the "Program" or "Write Enable" line tied to +5 Vdc which prevents the user from accidentally reprogramming or writing into the EPROM. The "Chip Select" logic is generated from decoder PROM U3 with separate output enable lines for each of the three EPROM memories.

c. EPROM Addressing. The CPU generates an address which is applied to all five memory devices (3

EPROM's and 2 RAM's). Through decoding portions of the address and CPU status lines, the desired EPROM or RAM is enabled. The applied address causes the corresponding 8-bit byte to appear on the output data bus (AD0-AD7). The CPU reads the byte via the BIU and processes this data along with other data to generate the desired CPU response.

d. EPROM Read and Write. Write operations are not allowed with EPROM's. If the CPU attempts to write to an EPROM, decode logic will prevent a memory select from occurring. An EPROM read operation consists of the following steps:

(1) An address is applied to inputs A0-A13.

(2) Both enables are at logic 0 ("read" and "memory select").

(3) The 8-bit byte corresponding to the applied address is placed on output terminals O0-O7, i.e., on the data bus.

(4) The "read" enable and memory select from the CPU and decoders go to logic 1, floating the data bus.

e. RAM Devices. Memory devices U19 and U20 are used for temporary and long term storage of data in support of the CPU software execution. Data may be read to and from the RAM's with "read" and "write" enable signals. The format of the RAM's is 2Kx8. The eleven address lines allow the selection of 2,048 (2K) 8-bit words. For example, an input address 101 1110 0001 may yield an output 8-bit byte 1011 1001. The RAM is addressed via the address bus and output 8-bit data is put on the 8-bit data bus.

f. RAM Read and Write Enables. The "write" enable is from the CPU. A logic 0 is "write" and a logic 1 is "read". Two enables are used; "RAM Select" and "Write enable" (both previously discussed). The "Write Enable" line is at logic 0 except during an microprocessor reset cycle.

g. RAM Read Cycle. A RAM read operation consists of the following steps:

(1) An address is applied to inputs A0-A10.

(2) Enables are both at logic 0.

(3) The Read/Write bit is set at logic 1, i.e., "read."

(4) The 8-bit byte corresponding to the applied address is placed on data terminals D0-D7, i.e., on the data bus.

(5) The "RAM Select" enable goes to logic 1, clearing the data bus.

h. RAM Write Cycle. A RAM write operation consists of the following steps:

(1) An address is applied to inputs A0-A10.

(2) Enables are both at logic 0.

(3) The Read/Write bit is set logic 0, i.e., "write."

(4) The status of the data bus AD0-AD7 is written into the RAM address via terminals D0-D7.

(5) The "RAM Select" enable goes to logic 1, isolating the RAM from the data bus.

i. RAM Supply Voltage. The volatile RAM memory devices are always powered and therefore retain all programming information, last operating parameters, BFO setting, etc. The RAM memory lithium battery supplies RAM power when the transceiver is not connected to a power source. The lithium battery has a nominal life of 10 years. RAM devices U19 and U20 are powered by +5 Vdc voltage regulator VR3 when primary power is applied to the transceiver, and by +3.6 Vdc battery BT1 when the transceiver is unpowered. A resistor (R24) in series with battery BT1 prevents excessive current draw if there is a fault on the board or if the battery voltage line is accidentally shorted to ground. Steering diodes CR2, CR4 and CR5 isolate each of the voltage sources. Diode CR3 is connected to the "common" terminal of VR3 to compensate for the diode voltage drop of the steering diodes CR2 and CR5. The output of VR3 is used by the CPU power-up circuit as a threshold voltage (Vth) and after power-up as a reference voltage. The RAM supply voltage is sampled and designated voltage standby (Vstby). Vstby is used in conjunction with the U14 bilateral switch which places either a ground or a + Vdc (Vstby) on the "Write Enable" logic line.

j. RAM Memory Erase. The RAM devices, which hold all channel programming information, last operating parameters, BFO frequency, etc., can be

erased totally by use of the memory erase push button located on the rear panel of the 100 Watt Transceiver. Typically, the erase button is used for security reasons when an unattended 100 Watt Transceiver is erased to prevent disclosure of operating frequencies, parameters, etc. The erase pushbutton, connected at J4, is normally closed, allowing the RAM voltage source to pass through the switch to U19 and U20. When the pushbutton is pressed, the voltage is removed from the RAM and the RAM voltage terminals are connected to ground via resistor R68. The ground path for the RAM voltage terminals eliminates any residual voltage held by the RAM and assures complete RAM erasure. Note that disconnection of jack J4 will also erase the RAM devices. If this is not desired, connect a jumper between terminals E12 and E13 before disconnecting J4. The memory erase function should only be used when absolutely necessary.

5-67. ANALOG-TO DIGITAL/DIGITAL-TO-ANALOG CONVERSION. A number of analog status and control voltages are converted to digital signals by the Analog-to-Digital converter U7. Signals converted from analog-to-digital are typically used for front panel digital displays. The RF GAIN parameter is converted from analog-to-digital by U7 and then converted by U22 from digital back to analog. The RF GAIN signal passes through this dual conversion to allow compatibility when the 100 Watt Transceiver is operated in the remote control mode. Conversion from analog-to-digital results in an 8-bit digital word that is stored in RAM until such time that the CPU requires its use.

a. Analog-to-digital converter U7. Refer to figure 5-23. Analog-to-digital converter U7 has eight analog inputs, I0-I7. The input that is to be converted is selected by BCD code on terminals A0-A2. A command "A/D Converter-Write" starts the A/D conversion, and at the end, "End of Conversion" logic is generated by U7. The 625 KHz used for the conversion process is generated from the 15 MHz crystal oscillator as discussed previously. The 8-bit digital output is routed to the data bus via buffer U34.

(1) The analog signals converted by U7 are:

(a) +15/-15 Vdc Balance (V BAL). A center-tapped voltage divider between the +15 and -15 Vdc supplies and ground is monitored. Nominally, the voltage between the two supplies is zero volts. If one of the supplies becomes unbalanced with respect to the other supply, the A/D conversion will indicate the difference, with the CPU taking appropriate action.

(b) Low Power Indicator (LOW PWR IND). The forward RF power sample is converted into a DC voltage and converted into a digital signal. If the incoming signal is greater than 1 volt and the transceiver is keyed and not tuning, the CPU will respond by illuminating the front panel LOW POWER indicator.

(c) Received Signal (V SIG). The receiver AGC voltage is processed to generate an analog signal which is converted into digital to illuminate front panel meter segments (S Scale). The stronger the receiver signal, the more segments are illuminated.

(d) Forward Power (V FWD). The forward power discriminator sample is processed to generate an analog signal which is converted into digital to illuminate front panel meter segments (1-150 Scale). The higher the transmit power level, the more segments are illuminated.

(e) Reflected Power (V REFL). The reverse power discriminator sample is processed to generate an analog signal which is converted into digital to illuminate front panel meter segments (1-150 scale). The higher the reflected power, the more meter segments are illuminated.

(f) Audio Frequency Shift Keying Center Frequency (V AFSK). A discriminator circuit generates an analog output proportional to the relative center frequency of the received AFSK tones. This analog representation is converted to a digital signal for application to the front panel meter. The digital output is further processed by the CPU to illuminate a single meter element showing left, right, or center AFSK frequency.

(g) Audio Level (V AUDIO). An audio sample from the selected audio source is processed and converted to digital for front panel meter display. The higher the audio power, the more meter segments are illuminated. The meter uses the scale -20 to +10 dBm.

(h) RF Gain (RF GAIN). An analog voltage is generated from the front panel RF GAIN control. However, it is first converted into a digital signal and then converted back to an analog signal because RF GAIN is also used in the remote control mode. When operating in remote, the RF GAIN signal is converted

to digital at the remote location for the serial data link and then re-converted to analog at the transceiver location.

(2) The desired A/D U7 input (I0-I7) is selected by the address bits A0-A2 in BCD code:

A2	A1	A0	Convert	
0	0	0	I0	RF GAIN
0	0	1	I1	V BAL
0	1	0	I2	LOW PWR IND
0	1	1	I3	V SIG
1	0	0	I4	V FWD
1	0	1	I5	V REFL
1	1	0	I6	V AFSK
1	1	1	I7	V AUDIO

(a) The conversion is enabled by the logic signal "Analog-to-Digital Converter - Write" from the U5 decoder. The clock signal for the conversion is the 625 KHz reference generated by divider circuits from the 15 MHz crystal clock. The CPU receives a status signal "End of Conversion" which goes to logic high at the end of the analog-to-digital conversion, indicating that the data at terminals D0-D7 is ready to be read. The data is read via buffer U34, which is enabled by "Analog-to-Digital Converter - Read". U34 allows fast read operations. (Using the U7 "Output Enable" would require additional data bus time.)

(b) Most of the data generated by A/D U7 is directed to the transceiver front panel meter. The 8-bit word generated by U7 is processed by the CPU with a software "look-up" table, which determines which meter scale segments should be illuminated. A logarithmic conversion is made in software for the -20 to +10 dBm scale used with audio source measurements.

b. Digital-to-Analog Converter U22. The U22 digital-to-analog converter is used only for the RF GAIN feature. Conversion from analog-to-digital is accomplished by U7; conversion back to analog is accomplished by U22. The current output of U22 is converted to voltage by OP AMP U39-A. The 0 to -5 Vdc output of U39-A is amplified by 2 and inverted by OP AMP U39-B, resulting in a final output of 0 to +10 Vdc for application to the RF GAIN control circuits. Capacitor C57 in the U39-B feedback path acts as a low pass filter to eliminate noise generated by the surrounding circuitry. The U22 digital-to-analog converter is enabled simultaneously with the U7 analog-to-digital converter using the select line "Analog-to-Digital Converter - Write". To prevent the RF GAIN level from being upset by a conversion other than RF GAIN, immediately following the strobing of gate U34 for the A/D conversion output the CPU program sends out the previous RF GAIN setting to keep the RF GAIN setting current.

5-68. INTERRUPT CONTROLLER U24. The CPU software routine is interrupted when the U24 interrupt controller detects a change in status signals. The CPU will then service the interrupt and then return to the routine it was executing. A substantial portion of CPU processing is handling of the interrupts. Many events in the transceiver are not monitored by a polling method; rather, the CPU waits to be informed of a change (interrupt) which is vectored to a software routine.

a. Interrupt Inputs. Refer to figures 5-24 and 5-25. There are eight interrupts associated with U24:

(1) RF Attention (RFATTN). An interrupt from one of the RF modules, indicating a need to be serviced or for a status to be processed by the CPU.

(2) RX Ready (RXRDY). An interrupt from the remote control unit for RX ready. The "RX" refers to a remote UART (Universal Asynchronous Receiver/Transmitter) integrated circuit and not to the receiver portion of the transceiver.

(3) TX Ready (TXRDY). An interrupt from the remote control unit for TX ready. The "TX" refers to a remote UART (Universal Asynchronous Receiver/Transmitter) integrated circuit and not to the transmitter portion of the transceiver.

(4) RX Ready - Auxiliary (RXRDYa). An interrupt from the remote control unit for RX ready-Aux. The "RX" refers to a remote UART (Universal Asynchronous Receiver/Transmitter) integrated circuit and not to the receiver portion of the transceiver. This interrupt is for expansion and is not used.

(5) Real Time Clock (RTC). The Real Time Clock runs continuously and interrupts the CPU every 13.1072 milliseconds.

(6) Front Panel Attention (FPATTN). An interrupt from the front panel keyboard, indicating that a button has been pushed by the operator.

signal going from logic low to logic high, i.e., the positive leading edge causes the interrupt. The keyline could be in any mode of operation and is called the unprocessed or "raw" keyline. The CPU operates in conjunction with interrupt 6 to follow the status of the keyline opening and closing.

(8) Raw Key ($\overline{\text{RAW KEY}}$). This interrupt indicates that a keyline has been opened by the status signal going from logic low to logic high, i.e., the positive leading edge causes the interrupt. The keyline could be in any mode of operation and is called the unprocessed or "raw" keyline. The CPU operates in conjunction with interrupt 7 to follow the status of the keyline opening and closing.

b. Interrupt Timing. Interrupts may occur at any time in the CPU software program. When an interrupt occurs, the CPU stops what it is doing, the CPU return address and flags are "pushed" onto a memory "stack" located in RAM, and the interrupt is vectored to the associated software routine and serviced. After the interrupt routine is completed, the CPU "pops" the information from the "stack" back into the CPU registers and the program picks up where it was before the interrupt occurred. U24 advises the CPU of an interrupt through the "Interrupt" status line connected directly to the CPU. The CPU, when ready to service the interrupt, responds through the "Interrupt Acknowledge" line. In processing the interrupt, data will "read" or "write" to the interrupt controller over the data port D0-D7.

c. Interrupt Read. During a "Read" function, the "Interrupt Controller-Read" logic is set, and the status of the eight interrupt lines appears on the data bus. For each interrupt, the interrupt controller provides a 'type' number, which the 8088 uses as a pointer to a vector in memory that is associated with the particular interrupt. If an interrupt is 'masked', then the 8088 does not receive an interrupt for that particular interrupt source. For example, a "Real Time Clock" interrupt may be masked in favor of a "Keyline" interrupt.

d. Interrupt Write. During a "Write" function, the "Interrupt Controller-Write" logic is set, and the CPU can write an eight bit word into the interrupt controller containing mode, type, and mask information. The interrupt controller then provides interrupts to the CPU to establish the preassigned priorities. Thus transceiver functions are prioritized during operation.

e. Typical Interrupt Read/Write Cycle. The address A0 applied to U24 acts in conjunction with the "Chip Select", "Read" and "Write" lines to decipher the data to and from the CPU. A typical interrupt sequence is as follows:

(1) One or more of the eight interrupt lines (I0-I7) are raised to logic high, setting the corresponding bits in the internal interrupt controller "Interrupt Request Register" (IRR).

(2) The interrupt controller evaluates these requests, and sends an "Interrupt" to the CPU, if appropriate.

(3) The CPU acknowledges the "Interrupt" and responds when ready with an "Interrupt Acknowledge" pulse.

(4) Upon receiving an "Interrupt Acknowledge", the controller internal "In Service Register" (ISR) highest priority bit is set and the corresponding IRR bit is reset. The interrupt controller does not drive the data bus during this cycle.

(5) The CPU initiates a second "Interrupt Acknowledge" pulse which releases an 8-bit "pointer" word onto the data bus, which is read by the CPU.

(6) This completes the interrupt cycle; the ISR bit is reset at the end of the second "Interrupt Acknowledge" CPU pulse.

(7) The CPU then decodes the interrupt controller "pointer" and vectors it to a software routine for processing.

5-69. PROGRAMMABLE PERIPHERAL INTERFACE U32. Refer to figures 5-26 and 5-27. Communication with the transceiver front panel and RF modules takes place via the U32 Programmable Peripheral Interface and supporting decoders, shift/storage registers, flip flops, and parallel-to-serial converters. The data line between the control board and the modules and front panel is called the "Module Control Bus", or MCB. The primary function of the Programmable Peripheral Interface, U32, is to control the data exchange between the control board and modules connected to the MCB, including enabling data "read", "write", addressing, etc.

a. Programmable Peripheral Interface Device. U32 has 24 I/O pins that are programmed in three sections of 8 bits each; PA0-PA7, PB0-PB7, and PC0-PC7. The PA and PC pins are programmed to be outputs, and the PB pins are programmed to be inputs. The two address inputs A0 and A1 are used to select one of the 8-bit input/output ports:

A1	A0	Select	
0	0	PA	(Read - Outputs)
0	1	PB	(Write - Inputs)
1	0	PC	(Read - Outputs)
1	1	Bus Control	(Write - Input)

b. Module Control Bus (MCB) Addressing with PPI. The front panel modules and RF modules are addressed with outputs from port A, PA0-PA3 and PA4-PA7, respectively. With the 4-bit outputs, a maximum of 15 modules may be addressed. The corresponding I/O front panel or RF module/assembly has a decoder that enables the data/transmitter receiver when the correct code for the device is detected. The address code for each module/assembly is shown below:

HEX Module Address	Front Panel (AD3 AD2 AD1 AD0) PA7 PA6 PA5 PA4	RF Module (AD3 AD2 AD1 AD0) PA3 PA2 PA1 PA0	Module/Assembly
RF 0 F0	1 1 1 1	0 0 0 0	Synthesizer Module
RF 1 F1	1 1 1 1	0 0 0 1	Receiver Module
RF 3 F3	1 1 1 1	0 0 1 1	AFSK Module
RF 4 F4	1 1 1 1	0 1 0 0	Reference/BFO Module
RF 5 F5	1 1 1 1	0 1 0 1	Exciter Module
RF 6 F6	1 1 1 1	0 1 1 0	LPA/Coupler Interface (W)
RF 8 F8	1 1 1 1	1 0 0 0	Reference/BFO Module
RF 9 F9	1 1 1 1	1 0 0 1	AGC/TGC Module
RF A FA	1 1 1 1	1 0 1 0	LPA/Coupler Interface(R)
RF B FB	1 1 1 1	1 0 1 1	AFSK Module
RF E FE	1 1 1 1	1 1 1 0	LPA/Coupler Interface
FP 2 2F	0 0 1 0	1 1 1 1	Front Panel - Frequency
FP 6 6F	0 1 1 0	1 1 1 1	Front Panel - Meter
RF/FP F FF	1 1 1 1	1 1 1 1	No Module Select

Notes

1. Only one front panel module is accessed. However, for software purposes, the entire 8 bit address strobe is considered.

2. (R) = Read Only; (W) = Write only. All others are Read and Write addresses. An underline indicates the function selected or affected by the action of the data strobe.

c. RF MCB Addressing by Destinations. Some assemblies have multiple functions and more than one assigned address. To clarify the destination of the data, the information above can be rearranged as follows:

(AD3 AD2) PA3 PA2		(AD1 AD0) PA1 PA0		Data Destination
0	0	0	0	Synthesizer Module
0	1	0	0	Reference/BFO Module - BFO Portion
1	0	0	0	Reference/BFO Module - Reference Portion
1	1	0	0	(Not Used)
0	0	0	1	Receiver Module
0	1	0	1	Exciter Module
1	0	0	1	AGC/TGC Module -TGC Portion
1	1	0	1	(Not Used)
0	0	1	0	(Not Used)
0	1	1	0	LPA/Coupler Interface -Coupler "Write"
1	0	1	0	LPA/Coupler Interface -Coupler "Read"
1	1	1	0	LPA/Coupler Interface -LPA Portion
0	0	1	1	AFSK Module -Keyer/Converter Portion
0	1	1	1	(Not Used)
1	0	1	1	AFSK Module -Frequency Offset Portion
1	1	1	1	(Not Used)

d. MCB Read and Write Cycles. Through CPU control, the U32 interface "writes" in an 8-bit word, via the data bus D0-D7, which then appears at the PA0-PA7 or PC0-PC8 terminals. In a similar manner, inputs to U32 that appear at the PB0-PB7 terminals form an 8-bit word that is read into the CPU on the data bus D0-D7 during a "read" sequence.

e. MCB Clock Generation. Although U32 receives no clock input, timing is generated for the clocking of serial data to and from the I/O ports. Since the timing involves the reading and writing of 8 bits of information, the clock runs for only 8 cycles. This clock is generated by an input of 2.5 MHz into dual flip flop U29. In order to run the clock for 8 cycles, the "Module Control Bus Data - Write" state goes to logic low, which enables a parallel load at parallel-to-serial converter U28. The 8-bit parallel load is all logic 1's since the U28 D0-D7 parallel inputs are all tied to the +5 Vdc line. The logic 1's then appear at the U28 Q7 output with Q7 going to logic 1 and Q7-not going to logic 0. The Q7-not line logic low provides the U28 enable, and the Q7 logic high removes the reset from dual flip-flop U29. With the reset removed from U29, the input 2.5 MHz clock is divided by 2 with U29-A to 1.25 MHz and then divided again by U29-B for an output of 625 KHz. Each output pulse of U29-B clocks the U28 serial output by 1 bit out of the U28 Q7 ports. The sequence is:

	U28 Outputs							
U29-B Flip Flop Pulse	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1
2	0	0	1	1	1	1	1	1
3	0	0	0	1	1	1	1	1
4	0	0	0	0	1	1	1	1
5	0	0	0	0	0	1	1	1
6	0	0	0	0	0	0	1	1
7	0	0	0	0	0	0	0	1
8	0	0	0	0	0	0	0	0

NOTE

Only Q7 is available as an output.

As shown above, after eight U29-B output pulses, U28 clocks out a logic zero, which holds flip flop U29 in reset and disables parallel-to-serial converter U28. This condition remains in effect until "Module Control Bus Data - Write" again goes to logic low and the cycle repeats.

f. MCB Clock Output. The eight output pulses are applied to U31 Shift/Storage register and to U33-B Decoder. The pulses are used on the "Enable" pin of U33-B. When the decoder input A0 is set to logic low ("RF Module" selected), clocking the "enable" pin results in a corresponding output called "RF Clock". When decoder input A0 is set to logic high ("Front

Panel" selected), clocking the "enable" pin results in a corresponding output called "FP Clock". The clock signal sent to the front panel or RF modules is used to clock serial data in and out to the assemblies.

g. MCB Data Registers. The eight 625 KHz pulses are also applied to the U31 shift/storage data register. This register reads in a serial word from an I/O port to create an 8-bit parallel word for the CPU or takes an 8-bit parallel word from the CPU and writes it out in serial form to an I/O port. I/O port data is either from the Front Panel, "FP Data In/Out", or from the RF Modules, "RF Data In/Out". Eight-bit serial data from the MCB is clocked into U31 by the U33-B "RF" or "FP" clock. The "FP Data In/Out" and "RF Data In/Out" data signals are disabled by the control line "MCB In/Out" at U30A-15. The AND gate U38-B combines the data paths into a single path. When data is coming in on one path, the other path is logic high, enabling AND U38-B. A "write" or "read" logic line from U32 is set for the "RF" or "FP" bus at PC4 and PC5, respectively.

h. MCB Data Read. Since there are exactly eight "FP" or "RF" clock pulses, the input data just fills the registers of U31. A command to read the U31 register into the CPU, "Module Control Bus Data - Read", is applied to the U31 "Output Enable" pin and the data reads to the CPU an 8-bit parallel word over the data bus.

i. MCB Data Write. In the opposite direction, when an 8-bit word from the CPU writes to the front panel or RF modules, the desired 8-bit word is placed on the data bus and then loaded into the U31 register. The load is accomplished by an enable signal generated from ANDing "Module Control Bus Data - Write" and "Out". Both of these signals are inverted before application to AND U38-A to obtain the correct sense. U31 is then clocked with 8 pulses of 625 KHz with the input parallel word being clocked out serially at U31 port Q7, starting with bit Q7 and ending with bit Q0. A larger number of write data bits than eight simply require the procedure to be repeated until the required number exits the Control Board.

j. FP or RF MCB Selection. The CPU selects either the front panel "FP" or RF modules "RF" as the destination for the 8-bit word and sets the input of decoder U33-A A0 accordingly. If A0 is set at logic low, the data destination is "RF". If A0 is set at logic high, the data destination is "FP". The output serial data from U31 pin Q7 is used as the "enable" signal for U33-A. As the data changes state, U33-A is alternately enabled and disabled and the data appears at the output of U33-A on either the "FP" or "RF" port, depending on the logic set at U33-A pin A0. The same "Out" logic used to load the parallel word into shift/storage register U31 enables buffer U30 and the serial data is clocked into the MCB.

5-70. LPA/COUPLER INTERFACE PWB ASSEMBLY A1A13, 10085-7000. This manual portion describes the LPA/Coupler Interface PWB as an individual assembly. Section I of this chapter describes the function of the LPA/Coupler Interface PWB in relation to overall 100 Watt Transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram	Figure 5-28
b. Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
f. Overall Interconnection	Figures FO-11 and FO-12
g. Transceiver Assembly Schematic Diagrams	Depot Manual

5-71. OVERALL LPA/COUPLER INTERFACE PWB FUNCTION. The function of the LPA/Coupler Interface PWB is to interface the 100 Watt Transceiver data, status, and control lines with an external 100/500 Watt or 1000 Watt Antenna Coupler and a 500 Watt or 1000 Watt LPA (Linear Power Amplifier). The primary inputs to the PWB are the MCB data, clock, and address signals.

a. Coupler Interface. The interface is accomplished with a series of buffered status control lines to and from the antenna coupler. The control lines include the following:

Control Lines to Antenna Coupler	Control Lines from Antenna Coupler
Coupler Bypass (100/500 Watt Antenna Coupler only)	Coupler Fault Coupler Over Temperature Coupler Tune Power Request Coupler Key Disable

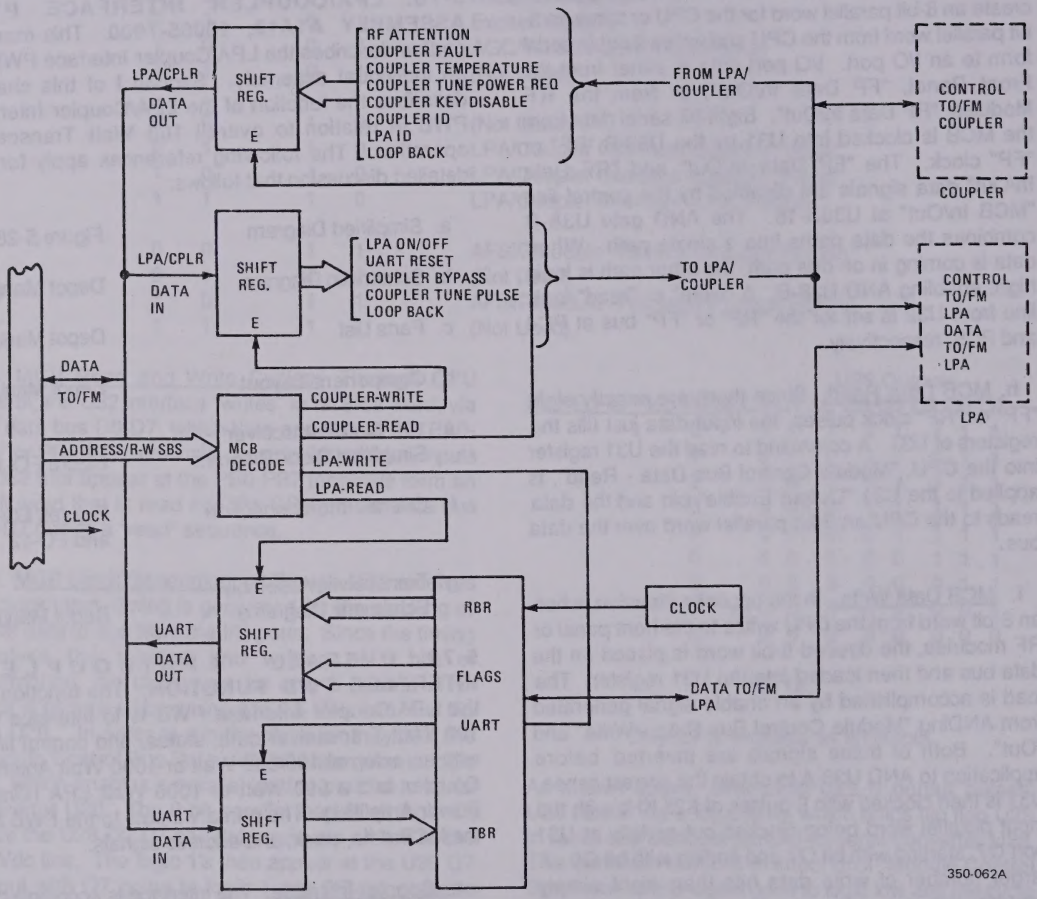


Figure 5-28. Simplified LPA/Coupler Interface

Coupler Tune Pulse	Coupler Identification

b. LPA Interface. The LPA interface consists of control lines and a bidirectional data interface for the exchange of control and status information. The data interface is via a Universal Asynchronous Receiver Transmitter (UART). A UART reduces noise pickup and reduces the number of control lines to be interfaced. The UART receiver converts serial data, start, parity and stop bits to parallel data, verifying proper code transmission, parity, and stop bits. The UART transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. All input/output 100/500 Watt Antenna Coupler and LPA connections are RFI decoupled by an inductor/capacitor to prevent RF from entering the PWB.

5-72. DETAILED LPA/COUPLER INTERFACE PWB BOARD CIRCUIT DESCRIPTIONS. The paragraphs below describe the LPA/Coupler Interface PWB assembly circuits. Each description heading begins with a device reference designation, e.g., Q1, Q2, etc., that identifies the circuit under discussion. The detailed information follows the signal flow shown on the LPA/Coupler Interface PWB Board schematic diagram.

a. MCB Interface U1, U6, U8, U10, U11, U12. Data from the A1A12 100 Watt Transceiver Control PWB is clocked into all RF module shift registers via the Module Control Bus (MCB). However, only one module receives the proper address to latch the data into its storage register. The 100 Watt Transceiver MCB interfaces with the LPA/Coupler Interface PWB and is assigned the following MCB addresses:

Decoded MCB Address:	AD3	AD2	AD1	AD0
Coupler-Write	0	1	1	0
Coupler-Read	1	0	1	0
LPA-Read/Write	1	1	1	0

b. MCB Decoding. When MCB data is intended for the LPA/Coupler Interface PWB, the decoding generates the desired enable signals for the bus registers. The clock signal shifts 8 serial bits of data into the U8 register if the Coupler-Write has been decoded, or into U12 if the LPA-Write has been decoded. After all data are clocked in, the WRITE strobe is decoded and the data in the bus registers are latched into the bus storage registers and appear at the bus register outputs as steady control voltages. The U1 decoding is as follows:

U1 Decoder Inputs			U1 Decoder Outputs	
(C) AD3	(B) AD2	(A) R/W	(Y)	
0	0	0	Y0	(Not Decoded)
0	0	1	Y1	(Not Decoded)
0	1	0	Y2	Coupler-Write
0	1	1	Y3	(Not Used)
1	0	0	Y4	(Not Used)
1	0	1	Y5	Coupler-Read
1	1	0	Y6	LPA-Write
1	1	1	Y7	LPA-Read

c. MCB Readback. Data from the LPA/Coupler Interface PWB to the control board is via 8-bit serial/parallel converter U6 for the Coupler-Read function, and via 16-bit serial/parallel converter U10/U11 for the LPA-Read function. The proper enable signals and "read" strobes are from the U1 decoder.

d. UART Transmitter Operation. The UART transmitter section accepts parallel data, formats it and transmits it in serial form on the TRO (Transmitter Register Output) terminal. Data is loaded into the transmitter buffer register from inputs TBR1-8 (Transmitter Buffer Register) by a logic low on the TBRL (Transmitter Buffer Register Load) input. The rising edge of TBRL clears TBRE (Transmitter Buffer Register Empty). One UART clock cycle after the data is loaded, TBRE is set high and serial data transmisison is started from port TRO (Transmitter Register Output). Output data is clocked by TRC (Transmitter Register Clock) with a clock rate 16 times the data rate. A high level on TRE (Transmitter Register Empty) indicates completed transmission of a character including stop bits.

e. UART Receiver Operation. Data is received in serial form at the RRI (Receiver Register Input) input. The RRI input is pulled high via resistor R16 when no data is being received. The data is clocked in by RRC (Receiver Register Clock) and is 16 times the data rate. A low level on DRR (Data Received Reset) clears the DR (Data Received) line. During the first stop bit, data is transferred from the receiver register to parallel output registers RBR1-8. One clock cycle later, DR is reset to logic high, and FE (Framing Error) is evaluated. A logic high on FE indicates an invalid stop bit was received and a framing error occurred. A

logic high on PE (Parity Error) indicates a parity error. A logic high on OE (Overrun Error) indicates the data received flag was not cleared before the last character was transferred to the received buffer register.

f. UART Master Reset Operation. The MR (Master Reset) input at high level clears the PE, FE, OE and DR to low level and sets the transmitter output to a high level after 18 clock cycles. MR does not clear the received buffer register. MR is generated by the input command UART RESET and during power-up. When power is first applied to the PWB, U7C-11 is held low until capacitor C63 is charged; MR is generated for approximately 100 milliseconds.

g. UART Data Interface.

(1) The UART is a bidirectional device with separate UART-transmit (TRO) and UART-receive (RRI) serial data ports. However, the TRO and RRI data streams are combined into a single serial data bus by opto-isolator U4 and transistor Q7, forming a current loop with a similar circuit in the LPA equipment. During UART-transmit, current is gated by transistor Q7, which is turned on and off by the data stream.

(2) During receive, transistor Q7 is always turned on. The input data then enables current to flow through opto-isolator U4, or stops the flow. The received data is inverted by U2-E, which in turn is enabled by RX ENABLE. RX ENABLE is generated from flip-flop U14A. U14A is cleared by LPA WRITE, which places a logic high on U14A-6. When the TRE (Transmitter Register Empty) occurs, the flip-flop U14A toggles, and a logic low appears at U14-6, i.e., RX ENABLE is generated when the transmitter register is empty.

h. UART Clock Generator. The UART clock signal is generated from 4.9152 MHz crystal oscillator Y1 and frequency divider U15. U15 has outputs of 1200, 2400, 4800 and 9600 baud. For operation of the 100 Watt Transceiver with the companion LPA's, the 4800 baud output is selected.

i. RF Attention. An RF Attention output is used as an interrupt signal at the A1A12 100 Watt Transceiver Control PWB. This causes the control board to service the interrupt as soon as possible. RF Attention is generated when the UART DR (Data Received) goes logic high, indicating a character has been received from the LPA and transferred to the receiver register, i.e., the UART is ready to read back a control word from the LPA. RF Attention is also generated when a Coupler Fault, Coupler Over Temperature, or TUNE POWER request is detected. NAND gate U7-6 output goes logic high whenever one of these conditions occurs. This logic high toggles flip-flop U14-B from a clear condition, and Q output U14-9 goes to logic high. This latches the fault condition until the control board can read the U6 data and determine the fault. The read cycle also clears U14- B.

j. Keyline Processing. The conditioned keyline input at J2-4 is logic low when the 100 Watt Transceiver is keyed. Transistor Q1 turns off, putting a logic high at the inputs of the inverter U5F and buffer U3E. The output of U3E exits the PWB as the LPA KEY. The output of U3E is enabled only when the output of U17B is logic low. The U17B output is logic low when a 100/500 Watt Antenna Coupler is not connected to the 100 Watt Transceiver or if a 100/500 Watt Antenna Coupler is connected and does not generate a KEY DISABLE* signal; the output is logic high when a 100/500 Watt Antenna Coupler is connected and it generates a KEY DISABLE*. The CPLR ID is brought to ground when the 100/500 Watt Antenna Coupler is connected.

* Indicates that the signal is active low. On schematic diagrams, active low signals have a bar over the top.

k. RF Mute. An RF MUTE command is generated when the 100/500 Watt Antenna Coupler KEY DISABLE is logic low. RF MUTE is used to prevent RF outputs from the 100 Watt Transceiver; however, RF MUTE does not cause the 100 Watt Transceiver to unkey. The KEY DISABLE control signal is inverted twice, by U17A and U5B, to develop the RF MUTE output. This output is further processed by U17C and U2, exiting the board at pins J2-3 and J3-28. RF MUTE from the LPA is wire ANDed with the 100/500 Watt Antenna Coupler KEY DISABLE. Therefore, either unit can generate an RF MUTE, which is connected directly to the Exciter PWB.

5-73. MULTIVOLTAGE CONVERTER ASSEMBLY A1A14, 10085-1240. This manual portion describes the Multivoltage Converter Assembly as an individual assembly. Section I of this chapter describes the function of the Multivoltage Converter Assembly in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Multivoltage Converter Simplified Diagram	Figure FO-9
b. Multivoltage Converter Schematic Diagram	Depot Manual
c. Voltage Regulator U2 Simplified Diagram	Figure 5-29
d. Parts List	Depot Manual
e. Component Layout	Depot Manual
f. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
g. Overall Interconnection	Figures FO-11,FO-12
h. Transceiver Assembly Schematic Diagrams	Depot Manual

5-74. OVERALL MULTIVOLTAGE CONVERTER ASSEMBLY FUNCTION. Multivoltage Converter Assembly A1A14 (part number 10085-1240) consists of two subassemblies: Multivoltage Converter PWB Assembly A1A14A1 (part number 10085-1260) and EMI Filter Assembly A1A14A2 (part number 10085-1230). The major function of the Multivoltage Converter Assembly is to power the low-level circuitry in the transceiver (except for the 100 Watt Power Amplifier Assembly). To do this, the assembly develops +/-15 V and +5 V from a +10 to +32 Vdc input, using a push-pull switching power supply and a series-pass switching power supply.

5-75. DETAILED MULTIVOLTAGE CONVERTER ASSEMBLY CIRCUIT DESCRIPTION. Refer to simplified diagram, figure FO-9, and the schematic diagram for this discussion. The power supply used in this equipment is a switching regulator. In basic operation, the input voltage is passed to the output filter as a train of pulses at a fixed repetition rate but with a controlled duty cycle. The duty cycle of the pulses is determined by the amount of error in the output voltage. The output filter network has a choke input and a flyback diode that allows the current through the choke to continue during the offtime of the pass transistors. The pulses are thus integrated to yield a dc voltage at the output of the filter. This output voltage is compared to a stable reference in the regulator. The result of the comparison controls the duty cycle of the pulses and thus controls the output voltge.

a. -15/+15 V Supply. The +10 to +32 Vdc input is first passed through EMI Filter FL1, a subassembly of the Multivoltage Converter Assembly. The output of FL1 then passes through choke L1 and is applied to Voltage Stabilizer Q1.

(1) Voltage Stabilizer Q1. Voltage Stabilizer Q1 maintains the power going into U1 and the driver stage (T1) at approximately +12 V. Once the power supply starts running, +15 V is fed back through CR1 to the emitter of Q1, so that the power supply runs on its own output.

(2) Pulse-Width Modulating Regulator U1. The +/-15 V supply is developed by a push-pull switching regulator, driven by Pulse-Width Modulating Regulator U1. (This pulse-width modulating regulator is also used on the +13.6 Vdc Power Supply PWB Assembly. Refer to paragraphs for the A2A2 +13.6 VDC Power Supply Assembly for a detailed description of this device.) The two outputs of U1 (CA at pin 12 and CB at pin 13) alternately drive transistors Q3 and Q4 to produce an ac current through the center-tapped primary of Driver Transformer T1. A bias current from the filtered Vdc line input is fed to the center tap via Voltage Stabilizer Q1 since T1 samples collector current to provide base drive. This bias current begins to turn the appropriate transistor on before the collector current builds up. When no drive is required to either Q8 or Q9, both Q3 and Q4 are on, shorting out T1.

(3) Driver Transformer T1. Driver Transformer T1 makes the transition from the low-level drive impedence to the transistor base impedence. T1 uses collector current feedback, with one turn of the secondary at the collector of Q8 and one turn at the collector of Q9, to provide an on-base current that is proportional to the collector current.

(4) Current Limit T2. The two primary leads of T3 are fed through transformer-coupled Current Limit T2. The outputs of T2 are then rectified by diodes CR10 and CR11. The network composed of Q7, R40, C13, R38, R39, C14, C39, and R44 provides the correct loop compensation at current limit input pin 4 of U1.

(5) Power Transformer T3. Transistors Q8 and Q9 alternately drive center-tapped Power Transformer T3. The leads of each secondary coil are fed to two full wave rectifiers, one for the +15 V output (CR12) and one for the -15 V output (CR16 and CR17). The output of CR12 is then filtered by

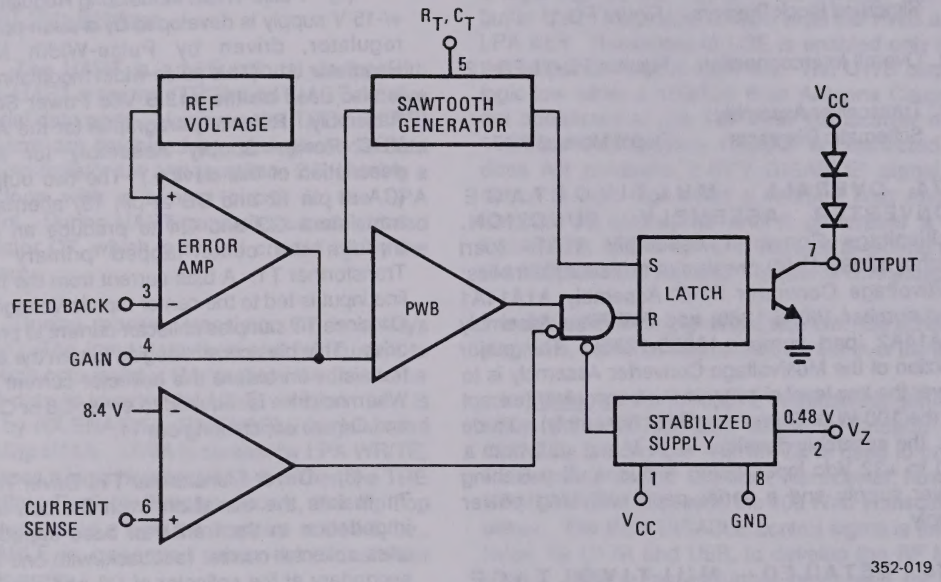


Figure 5-29. Voltage Regulator U2 Simplified Diagram

L2, C29 and C19. The -15 V line is filtered by L3 and C20. Both lines are then passed through EMI Filter FL1 and distributed to other assemblies in the transceiver.

(6) Output Voltage Feedback. The +15 V output is sampled at the input to FL1 and fed back through a voltage divider, which may be adjusted at potentiometer R4. The divided down feedback voltage is input to U1 at pin 1. In U1, the feedback voltage is compared to a reference voltage. The error is then used to determine the pulse-width of outputs at pins 12 and 13. The pulse-width controls the voltage level on the +15 V (and consequently -15 V) line.

(7) Under-Voltage/Over-Voltage Protection AR1. Voltage Comparators AR1-A and AR1-B provide under-voltage and over-voltage protection. AR1 shuts down U1 when line voltage is outside the range of +9 V to +35 V. The applied voltage is divided down by the voltage divider composed of R24, R28, and R32 and compared to a stable reference at the comparators. If the line voltage is outside these limits, the comparators drive soft start switch Q6 through common base stage Q12 reducing the control voltage to zero, resulting in the power supply shutting down.

(8) Soft-Start Switch Q6. Soft-Start Switch Q6 is driven by AR1A through common-base amplifier Q12. Q6, when turned on, discharges C7 through R37 reducing the control voltage to zero causing the regulator to shut down. When Q6 turns off, the 100 uA current source charges C7 resulting in a controlled rate of output voltage rise.

b. +5 V Supply. The filtered +10 to +32 Vdc input line also passes from choke L1 to circuitry that develops the +5 V supply. The +5 V supply is developed by a series-pass switching regulator, which is driven by Pulse-Width Modulating Regulator U2.

(1) Pulse-Width Modulating Regulator U2. Figure 5-29 is a simplified block diagram of U2. The output of U2 (pin 7) switches high and low to create a pulse at the base of Q11 (via Q13). The frequency of this pulse is determined by R51 and C25 (at pin U2-5). Circuitry in U2 compares feedback from the +5 V output line of the power supply to a reference voltage. U2 then adjusts the pulse-width at pin 7 according to the result of this comparison. The pulse-width determines the voltage level on the +5 V line.

(2) Current Transformer T4. When Q11 is enabled by U2 (via Q13), it drives Q10. From the secondary of current transformer, T4, which senses the Q10 collector current and provides a proportional Q10 base current, the collector current of Q10 is then sampled by the primary of current limit transformer T4.

(3) Current Limit Transformer T4. The one-turn primary of Current Limit T4 is at the collector leads of Q10 and Q11 to sense output current. The secondary of T4 is connected to current sense input U2-6 through the network of CR22, R49, R50, and C24. When the input at U2-6 begins to exceed the limit, circuitry in U2 decreases the pulse-width of the output at U2-7.

(4) +5 V Output and Feedback. From the primary of T4, the pulse from Q10 and Q11 is filtered by L4 and C21 and directed through to EMI Filter FL1. +5 V is then outputted from FL1 to other areas in the transceiver. A sample of the +5 Vdc is taken at the input to FL1 and fed back to U2. Before it is input to U2, this sample is divided down by a voltage divider that may be adjusted with potentiometer R61. The divided down sample is then input at feedback input pin 3. This feedback voltage is compared to an internal reference voltage. The amount of error in the feedback determines the pulse-width at output pin 7, which, in turn, controls the voltage level on the +5 V line.

(5) Under-Voltage/Over-Voltage Protection Q14. The +5 V switching power supply uses the same under-voltage/over-voltage protection circuit as the +15 V switching power supply. The output at the collector of Q6 controls the bias of Q14 via CR24 and R71. During shut-down, Soft-Start Switch Q6 is biased on, which biases Q14 on. Q14 pulls pin U2-4 to ground, which shuts down U2.

5-76. INTERCONNECT PWB ASSEMBLY A1A15, 10085-4210. This manual portion describes the Interconnect PWB as an individual assembly. Section I of this chapter describes the function of the Interconnect PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Schematic Diagram	Depot Manual
b. Parts List	Depot Manual
c. Component Layout	Depot Manual

d. 100 Watt Transceiver Simplified Block Diagram — Figure FO-1

e. Overall Interconnection — Figure FO-11, FO-12

f. Transceiver Assembly Schematic Diagrams — Depot Manual

5-77. OVERALL INTERCONNECT PWB FUNCTION. The purpose of the Interconnect PWB is to provide a common element for the interconnection of the various assemblies within the transceiver. The Interconnect PWB has a series of 11 jacks (J1-J8; J10-J12)) and 16 plugs (P1-P16). In addition, the Interconnect PWB contains an input power filtering network (C1, CR1, L1) and two supply voltage status indicators (DS1 for the +5 V and DS2 for the +13.6 V/+28 V DC IN).

5-78. AUDIO INTERFACE PWB ASSEMBLY A1A16, 10085-0570. This manual portion describes the Audio Interface PWB as an individual assembly. Section I of this chapter describes the function of the Audio Interface PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Schematic Diagram — Depot Manual

b. Parts List — Depot Manual

c. Component Layout — Depot Manual

d. 100 Watt Transceiver Simplified Block Diagram — Figure FO-1

e. Overall Interconnection — Figures FO-11, FO-12

f. Transceiver Assembly Schematic Diagrams — Depot Manual

5-79. OVERALL AUDIO INTERFACE PWB FUNCTION. The purpose of the Audio Interface PWB is to provide an interface between the transceiver rear panel terminal strip TB1 and certain audio functions associated with the Exciter and Receiver PWBs. TB1 is used for connection to telephone coupler units or external devices requiring audio (Line), and is directly soldered to the Audio Interface PWB. Additional TB1 connections include a push-to-talk keyline input, AGC monitor output, and signal ground. The Audio Interface PWB hybrid transformers convert separate transceiver receive and transmit audio pairs to and from a single 2-wire circuit. An output (J2) from the Audio Interface PWB provides audio connections to the remote control option if it is installed.

5-80. HYBRID TRANSFORMERS T1, T2, T3, T4. The audio connections to TB1 may be from 2-wire or 4-wire circuits.

a. 4-Wire Connections. When 4-wire connections are made, the following terminals are used:

TB1-1	Patch Audio Input - Balanced
TB1-2	Patch Audio Input - Balanced
TB1-3	Patch Audio Output - Balanced
TB1-4	Patch Audio Output - Balanced
TB1-5	Line Audio Input - Balanced
TB1-6	Line Audio Input - Balanced
TB1-7	Line Audio Output - Balanced
TB1-8	Line Audio Output - Balanced

b. 2-Wire Connections. When 2-wire connections are made to TB1, the following terminals are used:

TB1-1	(Not Used)
TB1-2	Patch Audio Input/Output - Balanced
TB1-3	Patch Audio Input/Output - Balanced
TB1-4	(Not Used)
TB1-5	(Not Used)
TB1-6	Line Audio Input/Output - Balanced
TB1-7	Line Audio Input/Output - Balanced
TB1-8	(Not Used)

c. 2-Wire/4-Wire Selection Switch. When input audio connections are from a 2-wire circuit, hybrid transformers are used to convert the input into a 4-wire circuit. The patch audio circuit uses transformers T1 and T2 with switch S1; T3 and T4 and switch S2 are used for line audio. Switches S1/S2 must be placed in the 2-wire or 4-wire position to match the audio connections. The hybrid balance is adjusted with R1/R5 to prevent crosstalk between the transmit

and receive audio signals during 2-wire operation. In addition to the 2-wire/4-wire conversion, T1-T4 convert the balanced audio connections at TB1 into 600 ohm unbalanced audio for use in the transceiver.

d. Relay K1. Relay K1 enables the PATCH input and output only when the PATCH audio source is selected on the transceiver front panel.

5-81. COUPLER CONNECTOR PWB ASSEMBLY A1A17, 10085-0550. This manual portion describes the Coupler Connector PWB as an individual assembly. Section I of this chapter describes the function of the Coupler Connector PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram	Figure 5-30
b. Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
f. Overall Interconnection	Figures FO-11, FO-12
g. Transceiver Assembly Schematic Diagrams	Depot Manual

5-82. OVERALL COUPLER CONNECTOR PWB FUNCTION. The Coupler Connector PWB is used to interface the rear panel COUPLER connector, J5, to the LPA/Coupler Interface PWB, A1A13. A simplified drawing of the Coupler Connector PWB is shown in Figure 5-30, and an overall schematic diagram is provided in the Depot Manual. Connections to the Coupler Connector PWB include:

J1	COUPLER connector J5, soldered directly to the PWB.
J2	Male connector pin for +13.6 Vdc connection.
E1	Ground lug for connection to the chassis.
J1-L	115 Vac-Line, soldered directly to the pin J1-L.
J1-M	115 Vac-Neutral, soldered directly to the pin J1-M.
W1	Cable assembly that connects W1P1 to LPA/Coupler PWB, A1A13. (W1P1 includes W1J1 which connects the LPA/Coupler PWB to rear panel LPA connector J8.)

5-83. AFSK ASSEMBLY A1A18, 10085-6000. This manual portion describes the AFSK Assembly (option) as an individual assembly. Section I of this chapter describes the function of the AFSK Assembly in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. AFSK Operation Simplified Diagram	Figure 5-31
b. AFSK Converter Timing Diagram	Figure 5-32
c. AFSK Schematic Diagram	Depot Manual
d. Parts List	Depot Manual
e. Component Layout	Depot Manual
f. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
g. Overall Interconnection	Figures FO-11, FO-12
h. Transceiver Assembly Schematic Diagrams	Depot Manual

5-84. OVERALL AFSK ASSEMBLY FUNCTION. As shown in figure 5-31, the AFSK Assembly consists of two primary circuits; the Keyer portion and the Converter portion. A teleprinter "space" and "mark" input and output DC voltages are converted or keyed into audio signals for radio transmission/reception. The Keyer circuits are used to convert input DC voltage levels representing "space" and "mark" into output audio tones for "space" and "mark". The Converter circuits are used to convert input audio "space" and "mark" tones to output DC voltage levels representing "space" and "mark". The radio transmission/reception of the TTY tones may be on upper or lower sideband (selectable), and there is a selection of three audio shift frequencies, as listed below. The sideband and

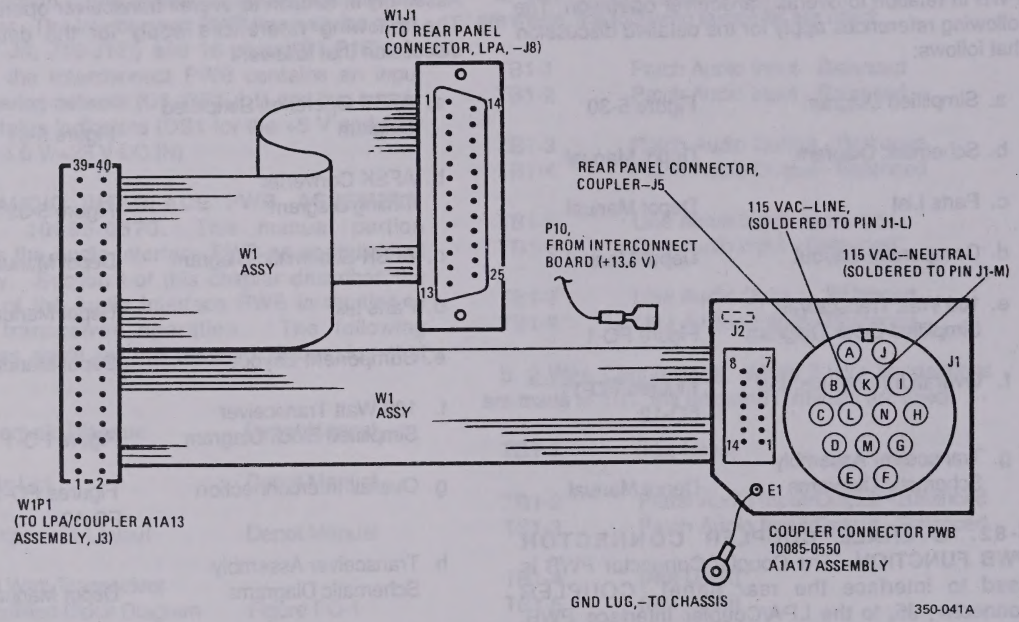


Figure 5-30. Simplified Diagram, Coupler Connector PWB

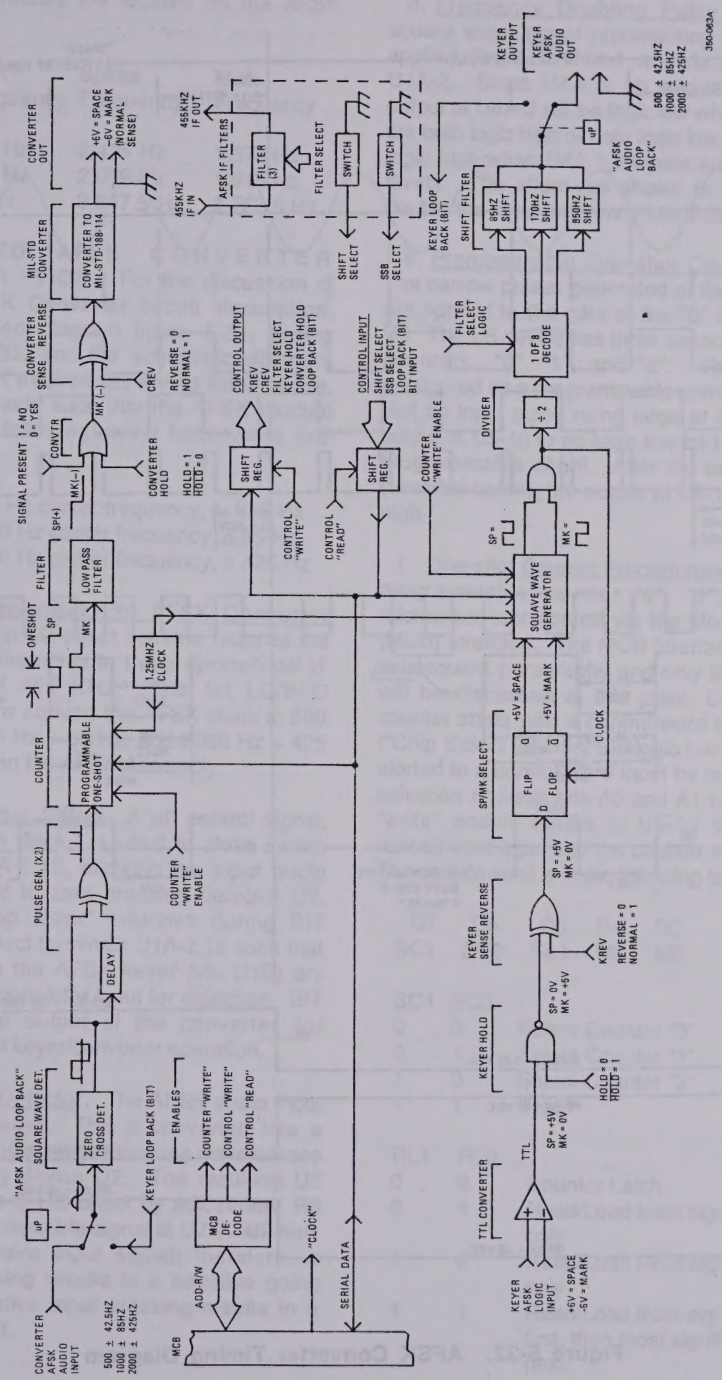


Figure 5-31. Simplified AFSK Operation Diagram

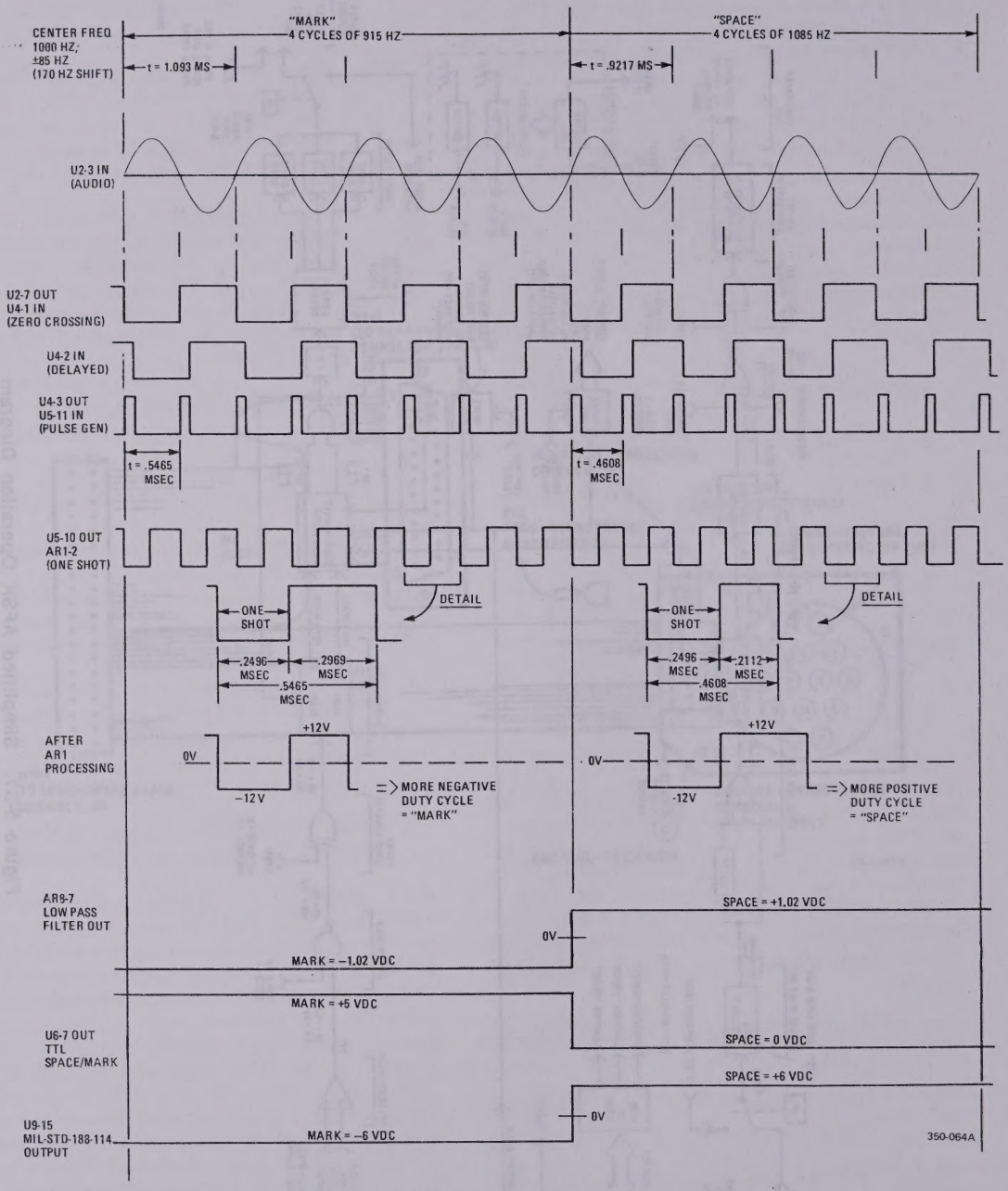


Figure 5-32. AFSK Converter Timing Diagram

shift selection switches are located on the AFSK Assembly.

Center Frequency	Shift Frequency	Space Frequency	Mark Frequency
2,000 Hz	850 Hz	2,425 Hz	1,575 Hz
2,000 Hz	170 Hz	2,085 Hz	1,915 Hz
2,805 Hz	85 Hz	2,847.5 Hz	2,762.5 Hz

5-85. DETAILED AFSK CONVERTER CIRCUIT DESCRIPTION. For the discussion of the detailed AFSK Converter circuit description, reference simplified diagram figure 5-31, timing diagram figure 5-32, and the schematic diagram. Although the AFSK frequencies are as listed above, conversions are made such that the AFSK module operates with the following center frequencies and shifts:

85 Hz Shift	500 Hz center frequency, ± 42.5 Hz
170 Hz Shift	1000 Hz center frequency, ± 85 Hz
850 Hz Shift	2000 Hz center frequency, ± 425 Hz

a. Frequency Processing for AFSK Converter Signal Inputs. A 1st LO offset scheme reduces the AFSK IF filter requirements to three symmetrical IF filters centered at 455 KHz. The 1st LO/BFO frequency selections convert the AFSK shifts to 500 Hz + 42.5 Hz, 1000 Hz + 85 Hz, and 2000 Hz + 425 Hz, for processing on the AFSK Assembly.

b. AFSK Converter Select. A uP control signal, "AFSK Audio Loop Back," is used to close switch U1A terminals U1A-1,15, allowing the input audio tones to be applied to zero crossing detector U2. "AFSK Audio Loop Back" switches during BIT sequencing to connect terminals U1A-2,15 such that audio outputs from the AFSK keyer (via U1B) are looped back to the converter input for detection. BIT then examines the output of the converter for verification of overall keyer/converter operation.

c. Zero Crossing Detector. The AFSK audio input is typically a sine wave. This is converted into a square wave by detecting when the sine wave passes through zero, using device U2. The resulting U2 square wave output is DC offset by adjustment R8 resulting in a TTL compatible signal at U2-7. U2 also inverts the sine wave input signal; therefore, a positive input crossing results in a negative going output, and a negative input crossing results in a positive going output.

d. Frequency Doubling Pulse Generator. The square wave signal representing the audio input is applied directly to U4A-1, and via a delay network to U4A-2. Since U4A is an exclusive-OR gate, the output at U4A-3 will be logic low when U4A-1,2 inputs are both logic high or both logic low, and U4A-3 will be logic high when U4A-1,2 inputs are at different logic levels. The effect, as shown in figure 5-32, is to double the input frequency into sharp, narrow pulses.

e. Programmable One-shot Counter Description. The narrow pulses generated at the output of U4A-3 are applied to the gate of the "0" counter portion of U5. The U5 device has three separate programmable counters, "0", "1", and "2". The "0" counter is configured as a programmable one-shot counter such that an input pulse rising edge at U5-11 causes the output at U5-10 to go logic low for the duration of the programmable count. After the one shot times out (terminal count), the output at U5-10 returns to logic high.

f. One-shot Counter Programming - Control. Each programmable counter "0", "1", "2", is under microprocessor control via the Module Control Bus (MCB) interface. The MCB interface is described in subsequent paragraphs and only the counter inputs will be discussed at this point. Control of the "0" counter starts with a control word input at U5-1 to 8 ("Chip Select" at U5-21 is logic low). The counter is alerted to a control word input by setting the counter selection address bits A0 and A1 to logic high. The "write" enable strobe at U5-23 then latches the control word input into the counter memory registers. The control word is in the following format:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL	M2	M1	M0	BCD

SC1	SC0	
0	0	Select Counter "0"
0	1	Select Counter "1"
1	0	Select Counter "2"
1	1	Illegal

RL1	RL0	
0	0	Counter Latch
0	1	Read/Load least significant byte only
1	0	Read/Load most significant byte only
1	1	Read/Load least significant byte first, then most significant byte next.

M2	M1	M0	
0	0	0	Mode 0 - Interrupt on Terminal Count
0	0	1	Mode 1 - Programmable One-shot
x	1	0	Mode 2 - Rate Generator
x	1	1	Mode 3 - Square Wave Generator
1	0	0	Mode 4 - Software Triggered Strobe
1	0	1	Mode 5 - Hardware Triggered Strobe

BCD	
0	Binary Counter 16 bit Format
1	Binary Coded Decimal (BCD) in 4 Decades

The "Select Counter" (SC) bits are set logic low for counter "0" selection; "Read/Load" (RL) bits are set logic high since one-shot counter programming requires 16 bits (2 bytes); "Mode" (M2, M1, M0) bits are set 0,0,1 respectively to select the programmable one-shot mode. The "BCD" control is set logic 1 which means the 16 bit programming inputs are divided into four 4-bit segments forming a 4-decade BCD counter. From this information, the control word is thus "33" in hexidecimal for selection of the "0" counter in a one-shot BCD configuration.

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD
0	0	1	1	0	0	1	1

|<----------"3"---------->| |<----------"3"---------->|

g. <u>One-shot Counter Programming - Timing.</u> After the control word has been loaded into the counter, as described above, the address A1/A0, "write", and "chip select" bits are set for selecting and loading the counter. The possible configurations are:

"Chip Select" CS	"Read" RD	"Write" WR	Address 1 AD1	Address 0 AD0	
0	1	0	0	0	Load Counter 0
0	1	0	0	1	Load Counter 1
0	1	0	1	0	Load Counter2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation
1	x	x	x	x	Disable
0	1	1	x	x	No Operation

Since we desire to load the counter "0" with one-shot programming, the control bits described above are set 0 1 0 0 0 respectively. At this time, data appears at U5 inputs D7 through D0 and is latched into memory as the first byte (least significant) for the one-shot programming. The "write" strobe is momentarily set in disable (logic high) while the next byte is loaded into U5 inputs D7 through D0. Again, the "write" strobe is set at logic low and the second byte (most significant) is latched into memory as the remainder of the one-shot programming.

h. <u>Programmable One-shot Counter Operation.</u> Once counter "0" is programmed with control and timing inputs, the U5 "chip select" line is set to logic high. This prevents any further programming commands, but has no effect upon the actual operation of the counter. Therefore, the counter now operates as a retriggerable one-shot where the rising edge of an input pulse at U5-11 gate causes the output at U5-10 to go logic low for the duration of the programming count. The actual duration of the one-shot is dependent on the 2-bytes (16 bits) loaded during the one-shot programming. This duration has three values, one for each of the three AFSK shifts. Remembering that the 16 bits were configured for BCD (4 decades), the configuration of the programming bytes is as follows:

|<----------2nd Byte----------->| |<----------1st Byte----------->|

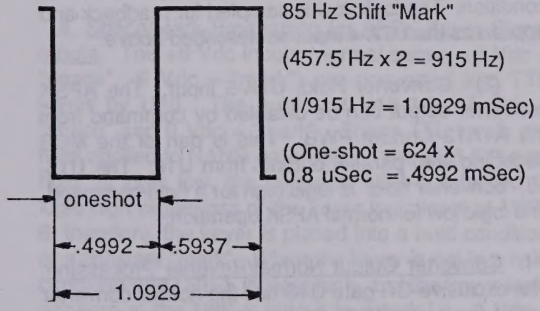
|<-------1000's------>| |<-------100's------>| |<--------10's-------->| |<---------1's---------->|

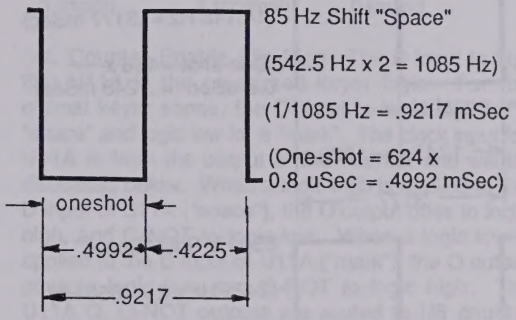
B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	
0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	0	85 Hz
0	0	0	0	0	0	1	1	0	0	0	1	0	0	1	0	170 Hz
0	0	0	0	0	0	0	1	0	1	0	1	0	1	1	0	850 Hz

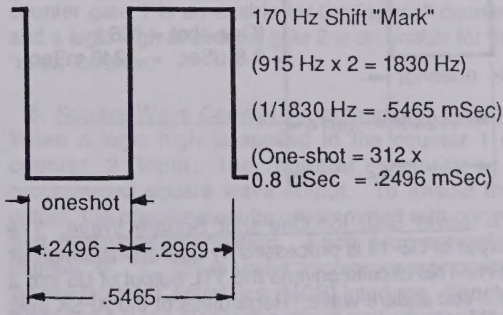
|<---------0---------->| |<---------6--------->| |<---------2--------->| |<--------4---------->| 85 Hz
|<---------0---------->| |<---------3--------->| |<---------1--------->| |<---------2---------->| 170 Hz
|<---------0---------->| |<---------1--------->| |<---------5--------->| |<---------6---------->| 850 Hz

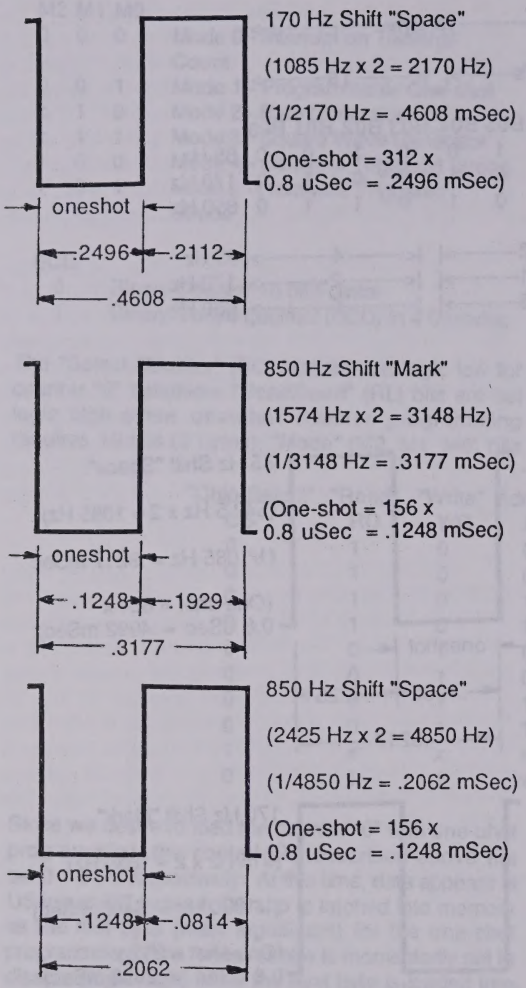
624 = 85 Hz Shift
312 = 170 Hz Shift
156 = 850 Hz Shift

Therefore, for the 85 Hz shift, the one-shot is programmed for 624 clock cycles, the 170 Hz shift for 312 clock cycles, and 850 Hz shift for 156 clock cycles. The U5 clock input is from oscillator Y1/U12 which is adjusted to 1.25 MHz with capacitor C22. Therefore, one clock cycle is equal to 0.8 uSec. Referring to the example in figure 5-32, the 170 Hz shift requires a one-shot duration of 312 clock cycles. This is calculated to be 312 x 0.8 uSec = .2496 mSec as shown. The one-shot duration is selected such that the duty cycle of the resultant square wave will average positive for a "mark" and average negative for a "space". In this manner, the outputs at U5-10 will be as follows for each one of the AFSK frequency shifts:









i. Level Shift for One-shot Square Wave. The output of U5-10 is processed by operational amplifier AR1. This circuit converts the TTL output of U5 into a ±12 Vdc square wave. Regardless of the AFSK shift selected, the duty cycle for a "mark" will be more negative, and the duty cycle for a "space" will be more positive (Note that the signal has been inverted relative to US-10). The 0 Vdc level for the square wave output is adjusted with R21.

j. Low Pass Filter. The processed square wave is applied to a series of active low pass filters using noninverting voltage followers. Only the average DC component appears at the last filter stage output at AR8-7; thus, the oscillating input is converted into DC level outputs. The value of the DC for "mark" and "space" varies with the AFSK frequency selection. For the 85 Hz and 170 Hz shift, a "mark" = -1.02 Vdc and a "space" = +1.02 Vdc; for the 850 Hz shift, a "mark" = -2.54 Vdc and a "space" = +2.54 Vdc.

k. Converter Output Enable Processing. The DC level outputs from the low pass filter are amplified and converted into TTL levels by U6. The U6-7 output is sampled for BIT sequencing readback, and is also applied to OR gate U7A-3. With the U7A-4,5 inputs at logic low, the AFSK transitions appear noninverted at U7A-6 output. However, if either of the U7A-4,5 inputs is at logic high, the U7A-6 output is held at logic high (a constant "mark") until the condition is cleared.

(1) Signal Present, U7A-4 input. The U7A-4 input is a "signal present" logic control signal derived from the output of AR3, which amplifies and inverts the AFSK RX AUDIO IN signal coming into J2-19. If the signal level is sufficient, the threshold level set by "threshold adjust" R73 for amplifier AR7 will be exceeded; and the output at AR7-1 will switch to +15 Vdc, indicating the received signal strength is adequate for AFSK operation. If the received signal strength is not sufficient, the output at AR7-1 is -15 Vdc. Diode CR7 blocks the negative outputs of AR7-1, and voltage divider R78/R79 reduces the positive output of AR7-1 to a TTL compatible level. Therefore, the input to inverter U21B is +5 Vdc, and the U21B output is logic low for a "signal present" condition. The logic low is sampled for readback and applied as the U7A-4 input as described above.

(2) Converter Hold, U7A-5 input. The AFSK converter output can be disabled by command from the A1A12 Control PWB. This is part of the MCB decoding with parallel outputs from U16. The U16-13, "converter hold" is logic high for a hold command, and logic low for normal AFSK operation.

l. Converter Output Normal/Reverse Processing. The exclusive-OR gate U4C has the normal converter sense input at U4C-8, i.e., "space" = logic low, and "mark" = logic high, and a control input at U4C-9, "Normal" = logic high, "Reverse" = logic low. Based on the exclusive-OR truth table, shown below, the converter sense is normal or reverse as determined by the control input. The operator sequence for selecting the Converter Reverse mode (CREV) is discussed in chapter 4 of this manual.

Converter Input U4C-8	Control Input U4C-9	Converter Output U4C-10
0 (space)	0 (reverse)	0 (space)
0 (space)	1 (normal)	1 (space)
1 (mark)	0 (reverse)	1 (mark)
1 (mark)	1 (normal)	0 (mark)

m. Converter MIL-STD-188-114 Output Processing. The normal/reverse converter output from U4C-10 is applied directly to the U9 tri-state dual differential line driver (only one used). U9 performs the function of converting the TTL input logic into the +6/-6 Vdc MIL-STD-188-114 output at U9-15. For the normal converter sense, the output is +6 Vdc = "space", and -6 Vdc = "mark". For the reverse converter sense, +6 Vdc = "mark" and -6 Vdc = "space".

5-86. DETAILED AFSK KEYER CIRCUIT DESCRIPTION. For the discussion of the detailed AFSK Keyer circuit description, reference simplified diagram, figure 5-31, and the schematic diagram. Although the AFSK frequencies are as listed in paragraph 5-84, conversions are made such that the AFSK module operates with the following center frequencies and shifts:

85 Hz Shift	500 Hz center frequency, ± 42.5 Hz
170 Hz Shift	1000 Hz center frequency, ± 85 Hz
850 Hz Shift	2000 Hz center frequency, ± 425 Hz

a. Space/Mark Processing for AFSK Keyer Signal Inputs. The +6 Vdc inputs (normal sense; +6 Vdc = "space", -6 Vdc = "mark") are converted into TTL levels by U10. The output at U10-2 is +5 Vdc = "space" and 0 Vdc = "mark". These TTL levels are then applied to NAND gate U8B. If the U8B-5 "keyer hold" is logic low, the output at U8B-4 is forced to logic high regardless of the keyer logic input at U8B-6; therefore, the keyer is placed into a hold condition of a constant "mark". When the keyer is not in a hold condition, the U8B-5 is logic high, and the keyer logic appears at the U8B-6 output inverted; i.e., 0 Vdc = "space", +5 Vdc = "mark". The "keyer hold" command is decoded from the MCB interface, via U16-5.

b. Keyer Input Normal/Reverse Processing. The exclusive-OR gate U4B serves to reverse the sense of the keyer input signal. Since input processing by NAND gate U8B inverts the keyer signal, the exclusive-OR gate U4B inverts for "normal" keyer sense, and does not invert for "reverse" keyer sense. The keyer inputs at U4B-6 are +5 Vdc = "mark" and 0 Vdc = "space", and the control input at U4B-5 is "normal" = logic high, and "reverse" = logic low. Based on the exclusive-OR truth table, shown below, the keyer sense is normal or reverse as determined by the control input. The operator sequence for selecting the Keyer Reverse mode (KREV) is discussed in chapter 4 of this manual.

Keyer Input U4B-6	Control Input U4B-5	Keyer Output U4B-4
0 (space)	0 (reverse)	0 (space)
0 (space)	1 (normal)	1 (space)
1 (mark)	0 (reverse)	1 (mark)
1 (mark)	1 (normal)	0 (mark)

c. Counter Enable Flip-Flop. The D input to flip-flop U11A is the processed keyer logic. For the normal keyer sense, the D input is logic high for a "space" and logic low for a "mark". The clock input for U11A is from the output of the counter and will be discussed below. When a logic high is applied to the D input of U11A ("space"), the Q output goes to logic high, and Q-NOT to logic low. When a logic low is applied to the D input of U11A ("mark"), the Q output goes to logic low, and Q-NOT to logic high. The U11A Q, Q-NOT outputs are routed to U5 counter gates 1 and 2 respectively. Therefore, a logic high at counter gate 1 is an enable for the "space" counter, and a logic high at counter gate 2 is an enable for the "mark" counter.

d. Square Wave Counter Programming - Control. When a logic high is applied to the counter 1 or counter 2 input, the counter generates a programmed square wave output. To enable this output, the counter must be programmed with control and frequency information. Each programmable counter "0", "1", "2", is under microprocessor control via the Module Control Bus (MCB) interface. Counter "0" is used in the Converter circuit and counter "1" is used for the generation of the "space" frequency and counter "2" is used for the generation of the "mark" frequency. The MCB interface is described in subsequent paragraphs and only the counter inputs will be discussed at this point. Control of the "1" and "2" counter starts with a control word input at U5-1 to 8 ("Chip Select" at U5-21 is logic low). The counter is alerted to a control word input by setting the counter selection address bits A0 and A1 to logic high. The "write" enable strobe at U5-23 then latches the

control word input into the counter memory registers. The control word is in the following format:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC1	SC0	
0	0	Select Counter "0"
0	1	Select Counter "1"
1	0	Select Counter "2"
1	1	Illegal

RL1	RL0	
0	0	Counter Latch
0	1	Read/Load least significant byte only
1	0	Read/Load most significant byte only
1	1	Read/Load least significant byte first, then most significant byte next

M2	M1	M0	
0	0	0	Mode 0 - Interrupt on Terminal Count
0	0	1	Mode 1 - Programmable One-shot
x	1	0	Mode 2 - Rate Generator
x	1	1	Mode 3 - Square Wave Generator
1	0	0	Mode 4 - Software Triggered Strobe
1	0	1	Mode 5 - Hardware Triggered Strobe

BCD	
0	Binary Counter 16 bit Format
1	Binary Coded Decimal (BCD) in 4 Decades

The "Select Counter" (SC) bits are set to logic 0,1 for counter "1" and 1,0 for counter "0". "Read/Load" (RL) bits are set logic high since counter programming requires 16 bits (2 bytes); "Mode" (M2, M1, M0) bits are set 0,1,1 respectively to select the square wave generator mode. The "BCD" control is set logic 1 which means the 16 bit programming inputs are divided into four 4-bit segments forming a 4-decade BCD counter. From this information, the control word is thus "77" in hexadecimal for selection of the "1" counter, and "B7" for selection of the "2" counter.

D7	D6	D5	D4	D3	D2	D1	D0	
SC1	SC0	RL1	RL0	M2	M1	M0	BCD	
0	1	1	1	0	1	1	1	Counter 1"space"
1	0	1	1	0	1	1	1	Counter 2"mark"

g. One-shot Counter Programming - Timing. After the control word has been loaded into the counter, as described above, the address A1/A0, "write", and "chip select" bits are set for selecting and loading the counter. The possible configurations are:

"Chip Select" CS	"Read" RD	"Write" WR	Address 1 AD1	Address 0 AD0	
0	1	0	0	0	Load Counter 0
0	1	0	0	1	Load Counter 1
0	1	0	1	0	Load Counter 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter 0
0	0	1	0	1	Read Counter 1
0	0	1	1	0	Read Counter 2
0	0	1	1	1	No Operation
1	x	x	x	x	Disable
0	1	1	x	x	No Operation

Since we desire to load the counter "1" with "space" programming, the control bits described above are set 0 1 0 0 1 respectively. At this time, data appears at U5 inputs D7 through D0 and is latched into memory as the first byte (least significant) for the square wave generator programming. The "write" strobe is momentarily set in disable (logic high) while the next byte is loaded into U5 inputs D7 through D0. Again, the "write" strobe is set at logic low and the second byte (most significant) is latched into memory as the remainder of the square wave generator programming. This same sequence is repeated for counter "2" with the control bits 0 1 0 1 0.

h. Programmable Square Wave Generator Operation. Once counters "1" and "2" are programmed with control and timing inputs, the U5 "chip select" line is set to logic high. This prevents any further programming commands, but has no effect upon the actual operation of the counters. Therefore, the counter now operates as a square wave generator whenever a logic high is applied to the gate 1 or gate 2 input. The frequency of the square wave output is dependent on the 2 bytes of frequency information loaded into the counter memory. For one-half of the frequency time, the output of the counter will remain logic high (for even numbers) and go low for the other half of the count. If the count is odd, the output will be high for (N+1)/2 counts and low for (N-1)/2 counts. This duration has six values, two for each of the three AFSK shifts. Remembering that the 16 bits were configured for BCD (4 decades), the configuration of the programming bytes is as follows:

|<----------2nd Byte----------->| |<----------1st Byte----------->|

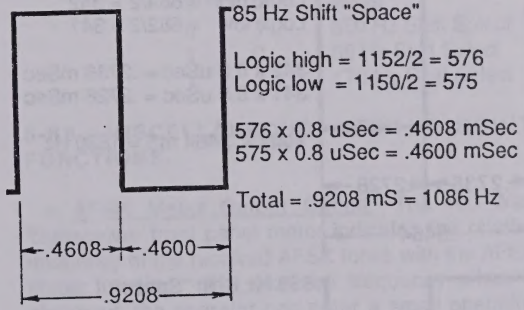
|<---1000's--->| |<---100's--->| |<---10's--->| |<---1's--->|

B15	B14	B13	B12	B11	B10	B09	B08	B07	B06	B05	B04	B03	B02	B01	B00	
0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1	85 Hz Sp
0	0	0	1	0	0	1	1	0	1	1	0	0	1	0	1	85 Hz Mk
0	0	0	0	0	1	0	1	0	1	1	1	0	1	1	0	170 Hz Sp
0	0	0	0	0	1	1	0	1	0	0	0	0	0	1	1	170 Hz Mk
0	0	0	0	0	0	1	0	0	1	0	1	1	0	0	0	850 Hz Sp
0	0	0	0	0	0	1	1	1	0	0	1	0	1	1	1	850 Hz Mk

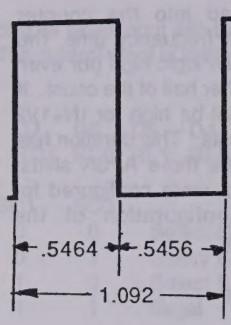
|<---1--->| |<---1--->| |<---5--->| |<---1--->| 85 Hz Sp
|<---1--->| |<---3--->| |<---6--->| |<---5--->| 85 Hz Mk
|<---0--->| |<---5--->| |<---7--->| |<---6--->| 170 Hz Sp
|<---0--->| |<---6--->| |<---8--->| |<---3--->| 170 Hz Mk
|<---0--->| |<---2--->| |<---5--->| |<---8--->| 850 Hz Sp
|<---0--->| |<---3--->| |<---9--->| |<---7--->| 850 Hz Mk

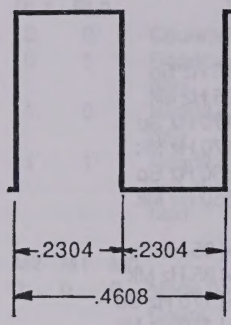
Therefore, the square wave generator programming is:

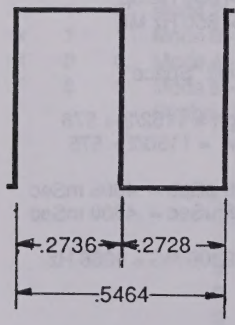
Clock Cycles	Shift	Sp/Mk
1151	85 Hz Shift	Space
1365	85 Hz Shift	Mark
576	170 Hz Shift	Space
683	170 Hz Shift	Mark
258	850 Hz Shift	Space
397	850 Hz Shift	Mark

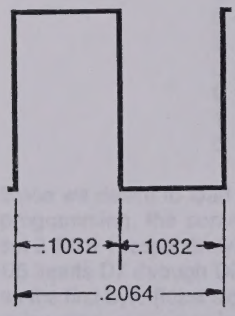


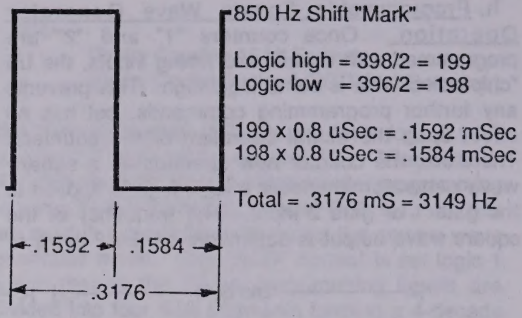
The U5 clock input is from oscillator Y1/U12 which is adjusted to 1.25 MHz with capacitor C22. Therefore, one clock period is equal to 0.8 uSec. For example, for the 170 Hz shift, space, there are 576 cycle cycles of 0.8 uSec each; and for 576/2 cycles, the output is logic high, and for 576/2 cycles, the output is logic low. Therefore, the output square wave is logic high for .2304 mSec and logic low for .2304 mSec, for a total of .4608 mSec, i.e., a square wave frequency of 2170 Hz. In this manner, the outputs at U5-13/17 will be as follows for each one of the AFSK frequency shifts:




170 Hz Shift "Space"
Logic high = 576/2 = 288
Logic low = 576/2 = 288
288 x 0.8 uSec = .2304 mSec
288 x 0.8 uSec = .2304 mSec
Total = .4608 mS = 2170 Hz
.2304
.2304
.4608




850 Hz Shift "Space"
Logic high = 258/2 = 129
Logic low = 258/2 = 129
129 x 0.8 uSec = .1032 mSec
129 x 0.8 uSec = .1032 mSec
Total = .2064 mS = 4845 Hz
.1032
.1032
.2064



i. Square Wave Output Processing. The output of U5 will either be a "space" or a "mark" as commanded by the U11A flip-flop. The frequency shift is determined by the counter programming via the MCB control, as described above. The resultant square wave output is applied to NAND U8A which inverts the square wave (the counter that does not have an output sits at logic high for the opposite U8A input), and U8D acts as inverter for the final square wave output at U8D-11. This output is sampled for the U11A clock, as described above, and is then applied to a divide-by-2 flip-flop U11B. U11B has "reset" logic such that a keyer output is generated at U11B-10 only when the 100 watt transceiver is in transmit and keyed. During periods of receive, or unkeyed transmit, there is no keyer output from U11B. If a BIT sequence has been enabled, the uP4 control line goes logic low, and a U11B-10 output is generated for testing purposes. After the U11B divide-by-2, the AFSK frequencies are:

1086/2	= 543 Hz	85 Hz Shift	Space
915/2	= 457.5 Hz	85 Hz Shift	Mark
2170/2	= 1085 Hz	170 Hz Shift	Space
1830/2	= 915 Hz	170 Hz Shift	Mark
4845/2	= 2422.5 Hz	850 Hz Shift	Space
3149/2	= 1574.5 Hz	850 Hz Shift	Mark

j. AFSK Tone Filters and Output. The square wave outputs of U11B are now filtered to generate the desired AFSK sine wave tones. The U13 1-of-8 decoder routes the square wave to one of the three AFSK tone filters, as determined by the U13 logic inputs A and B. The filter select logic is as follows:

S1 (B)	S0 (A)	Filter Selected
0	0	OFF
0	1	850 Hz
1	0	85 Hz
1	1	170 Hz

All of the tone filters are connected at a common node and applied to switch U1B. Switch U1B is normally closed, connecting terminals U1B-4,3. During BIT sequencing, the switch is operated by "AFSK Audio Loop Back" logic to connect terminals U1B-4,5 and thereby looping back the keyer output tones to the converter input (via U1A). The converter output logic is then examined by BIT to verify overall keyer/converter operation. The final selected AFSK tones exit the AFSK PWB at terminal J2-18.

5-87. AFSK PWB MCB INTERFACE. The control signals for the AFSK Assembly are read into the assembly in a serial data stream. The MCB address strobe is coded for two AFSK functions. The AD3-AD2-AD1-AD0 address for the AFSK U5 counter is 1011 (B); for AFSK control the address is 0011 (3). Only Write is decoded for the AFSK U5 counter programming, and both Read and Write are decoded for the AFSK control function. AD0 and AD2 are used as enables for 1-of-8 decoder U14, and AD1 and AD3 are used as decoder inputs along with the read/write strobe.

a. MCB Write. When MCB data is intended for the AFSK Assembly, the decoding generates the desired enables for the bus registers. The clock signal then clocks in serial bits of data into the U17/U18 shift registers, if the U5 counter programming "write" was decoded, or into U16 if the AFSK control "write" was decoded. The third data bit loaded during U16 "write" is used as part of the AFSK MCB loop back BIT test sequence (Q3 output). After all the data are clocked in, the "write" strobe is decoded and the data in the bus registers are latched into the bus storage registers and appear at the bus register output pins as steady control voltages. For the U5 counter operation, the decoded "write" strobe is routed to U5 as the input U17/U18 shift register strobe is tied directly to +5 Vdc for a constant enable. All the outputs of U17/U18 are utilized as discussed in previous paragraphs. The control outputs of U16 include the following:

U16 Outputs	Write Function
Q1	KREV (Keyer Reverse)
Q2	Keyer Hold NOT (BIT)
Q3	Loop Back (BIT)
Q4	AFSK Audio Loop Back (BIT)
Q5	CREV (Converter Reverse)
Q6	Converter Hold (BIT)
Q7	AFSK Filter Select S0
Q8	AFSK Filter Select S1

S1	S0	Filter
0	0	OFF - No Filter Selected
0	1	850 Hz Shift Filter
1	0	85 Hz Shift Filter
1	1	170 Hz Shift Filter

b. MCB Read. When AFSK data is to be read back to the Control PWB via the MCB, the decoding generates the desired "read" enable for the bus register of U15. During the microprocessor read function, the eight inputs to the parallel/serial register are read in serial to the Control PWB, although only six are used (P3-P8). The 8-bit byte consists of the following:

U15 Inputs	Read Function
P1	(Not used)
P2	(Not used)
P3	Signal Present NOT
P4	AFSK Sideband Select (1 = USB, 0 = LSB)
P5	MCB Loopback
P6	RX Data (1 = "Space", 0 = "Mark")
P7	AFSK Shift Select B0
P8	AFSK Shift Select B1

B1	B0	Select
0	0	Illegal
0	1	850 Hz Shift Select
1	0	85 Hz Shift Select
1	1	170 Hz Shift Select

5-88. MISCELLANEOUS AFSK CIRCUIT FUNCTIONS.

a. AFSK Meter Output Circuit. The 100 Watt Transceiver front panel meter indicates the relative frequency of the received AFSK tones with the AFSK Meter function. If a received frequency offset is observed, the operator can enter a small operating frequency correction to center the AFSK display and therefore the detected AFSK output. The AFSK display is accurate only when normal space/mark data is being received. A constant "space" or "mark" will give a false meter indication. The converter low pass filter output is sampled and applied to AR8 to generate the meter display. AR8 amplifies the RX data sample and looks for an imbalance in the data duty cycle between space and mark, i.e., the positive

and negative excursion of space and mark should be equally positive and negative; if not, an imbalance exists in the received frequency. The reference voltage for AR8 is adjusted with R86. Duty cycle imbalance results in the DC output at J2-21 to vary depending on the magnitude of the frequency error. The analog-to-digital and software processing of the AFSK meter voltage then illuminates the appropriate meter segment at the front panel meter display. The value of the low pass filter output sample is adjusted when the 850 Hz shift is selected by closing the switch U1C. This allows a constant shift voltage at the input to AR8A regardless of the AFSK operating frequency.

b. AFSK IF Filter Selection. The logic signals for selection of the AFSK IF Filter are generated from 1-of-4 decoder U20. The inputs to U20 are U16 control signals S0/S1. The filter selected is based on the following code:

U20 Out	S1	S0	Filter
Q0	0	0	OFF - No Filter Selected
Q1	0	1	850 Hz Shift IF Filter Select
Q2	1	0	85 Hz Shift IF Filter Select
Q3	1	1	170 Hz Shift IF Filter Select

When no filter is selected, OR-gate U7 and inverter U3 disable U20. Driver amplifiers invert the U20 outputs such that a driver voltage of -15 Vdc = Filter Select, and +15 Vdc = Filter Select-NOT. The filter control voltages exit the AFSK PWB and are routed to the AFSK Filter Assembly. At the AFSK Filter Assembly, filter selection is accomplished through the use of switching diodes. For example, if the 85 Hz shift filter is selected, the -15 Vdc control voltage turns on diodes CR1 and CR4, thus completing the circuit path for the IF input/output signal. The remaining filters have +15 Vdc applied back biasing the select diodes, plus shunt diodes are turned on to remove all IF signal from the unselected filter input/output. The AFSK filters are symmetrical and centered at 455 KHz with the following nominal 3 dB bandwidths:

850 Hz Shift	454.450 KHz - 455.550 KHz
170 Hz Shift	454.890 KHz - 455.110 KHz
85 Hz Shift	454.945 KHz - 455.055 KHz

c. BIT Testing. During BIT sequencing, the keyer portion of the AFSK PWB generates, under microprocessor control, all possible AFSK frequencies. Through the switching of U1, the keyer audio outputs are looped back to the converter input. The converter then detects the AFSK frequencies with a TTL sample at the RX data output of U6-7 being routed back to the microprocessor for verification (U15-14). The BIT keyer/converter hold logic is used to allow BIT testing when teleprinter equipment is connected to the AFSK, i.e., the teleprinter equipment will not be aware that BIT testing has taken place. However, BIT testing should not be enabled during the receiving or transmitting of normal AFSK traffic since there would be an interruption of the message.

d. Programmable Counter Clock Oscillator. The clock input for the programmable counter U5 is from oscillator Y1/U12. The oscillator output is enabled by application of +5 Vdc to the U12 power input. This is switched with transistor Q2 that has its base connected to the output of inverter U3F. When no AFSK filter is selected, the output of U3F is logic high, transistor Q2 is not turned on, and U12 is not powered, i.e., the oscillator output is disabled.

5-89. REMOTE CONTROL ASSEMBLY A1A19, 10088-6000. This manual does not supply information regarding the A1A19 Remote Control PWB, since it is a part of the Control Unit, Remote C-11329/URC. For information regarding the Remote Control PWB, refer to T.O. 31R2-2URC-91 (On-equipment) and 31R2-2URC-93 (Depot).

5-90. CONNECTOR PLATE ASSEMBLY A1A20, 10085-0580. This manual portion describes the Connector Plate Assembly as an individual assembly. Section I of this chapter describes the function of the Connector Plate Assembly in relation to overall transceiver operation. The only function of this assembly is to provide the interface connection between the 100 Watt Transceiver and the associated Power Supply. The following references apply for this assembly:

a. Schematic Diagram	Depot Manual
b. Parts List	Depot Manual
c. Component Layout	Depot Manual
d. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
e. Overall Interconnection	Figures FO-11 and FO-12

f. Transceiver Assembly Schematic Diagrams — Depot Manual

5-91. POWER SUPPLY UNIT A2, 10085-0200. This manual portion describes the Power Supply Unit as an individual assembly. Section I of this chapter describes the function of the Power Supply in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram Power Supply Unit — Figure 5-33

b. Schematic Diagram Power Supply Unit — Depot Manual

c. Parts List — Depot Manual

d. Component Layout — Depot Manual

e. 100 Watt Transceiver Simplified Block Diagram — Figure FO-1

f. Overall Interconnection — Figures FO-11 and FO-12

g. Transceiver Assembly Schematic Diagrams — Depot Manual

5-92. OVERALL POWER SUPPLY UNIT FUNCTION. The Power Supply Unit, A2, houses all "A2" designated transceiver modules. These modules are Power Supply Protection and Control Assembly A2A1, +13.6 Vdc Power Supply Assembly A2A2, and EMI Filter Assembly A2A3. In addition, Power Supply Unit A2 includes circuitry in the chassis itself. The Power Supply develops a single voltage output of +13.6 Vdc, from either a 110/220 Vac input or a +12/+28 Vdc input.

5-93. OVERALL TECHNICAL DESCRIPTION, POWER SUPPLY UNIT, A2. The paragraphs that follow describe how the Power Supply functions as a complete unit. Refer to figure 5-33 for this discussion. Detailed discussions about Power Supply Protection and Control Assembly A2A1 and +13.6 Vdc Power Supply Assembly A2A2 are given in paragraphs for these assemblies.

a. Dc Operation. To select dc operation, a dc line cord is connected to J1 and a 12 V or 28 V dc source is applied to pins J1-A (positive) and J1-D (negative). POWER ON/OFF Switch A1A11S2 (Front Panel Assembly) completes the loop between A2A1J4-6 (dc supply) and A2A1J4-5 (input to logic on A2A1). The +12/28 Vdc input enters the Power Supply Unit at J1-A. Circuit breaker CB3 protects the rest of the circuitry from current exceeding 50 amperes. DC ON/OFF Relay K1 is controlled by logic on the Power Supply Protection and Control Assembly. JMP1 and A2A1TB1 are configured for either a +28 Vdc or +12 Vdc power supply.

b. +12 Vdc Power Supply. A +12 Vdc input is routed from A2A1TB1 directly to EMI Filter Assembly A2A3, where it is rerouted to 100 Watt Assembly A1A4.

c. +28 Vdc Power Supply.

(1) From A2A1TB1, the +28 Vdc input is routed to step-start circuitry consisting of STEP-START Relay K2, resistors R3 and R1, control logic on the Power Supply Protection and Control Assembly, and 66,000 uF Filter Capacitor C1. From the step-start circuit the +28 Vdc is fed through the EMI Filter Assembly to +13.6 Vdc Power Supply Assembly A2A2.

(2) The +13.6 Vdc Power Supply Assembly converts the +28 Vdc to +13.6 Vdc, using a pulse-width modulating regulator. The +13.6 Vdc Power Supply Assembly is controlled by the SHUT-DOWN signal from Power Supply Protection and Control Assembly A2A1 and the CW/FSK signal initiated by mode selection on the transceiver front panel. A low on the CW/FSK line causes the +13.6 Vdc Power Supply Assembly to produce a reduced output voltage for better 100 watt PA efficiency.

(3) The output from +13.6 Vdc Power Supply Assembly A2A2 is filtered again on the EMI Filter Assembly (by A2A3L3 and A2A3L4). The EMI Filter Assembly filters noise that may be generated by the +13.6 Vdc Power Supply Assembly. The filtered +13.6 Vdc output leaves the Power Supply Unit via A3P1 and is routed to 100 Watt Assembly A1A4 as well as Multivoltage Converter Assembly A1A14.

d. AC Operation.

(1) Ac operation is selected by connecting an AC line cord to J1 pins B, E, and F (ground). POWER ON/OFF Switch A1A11S2 completes the loop between A2A1J4-1 (ac supply) and A2A1J4-3 (input to logic on A2A1). The 110/220 Vac input enters the

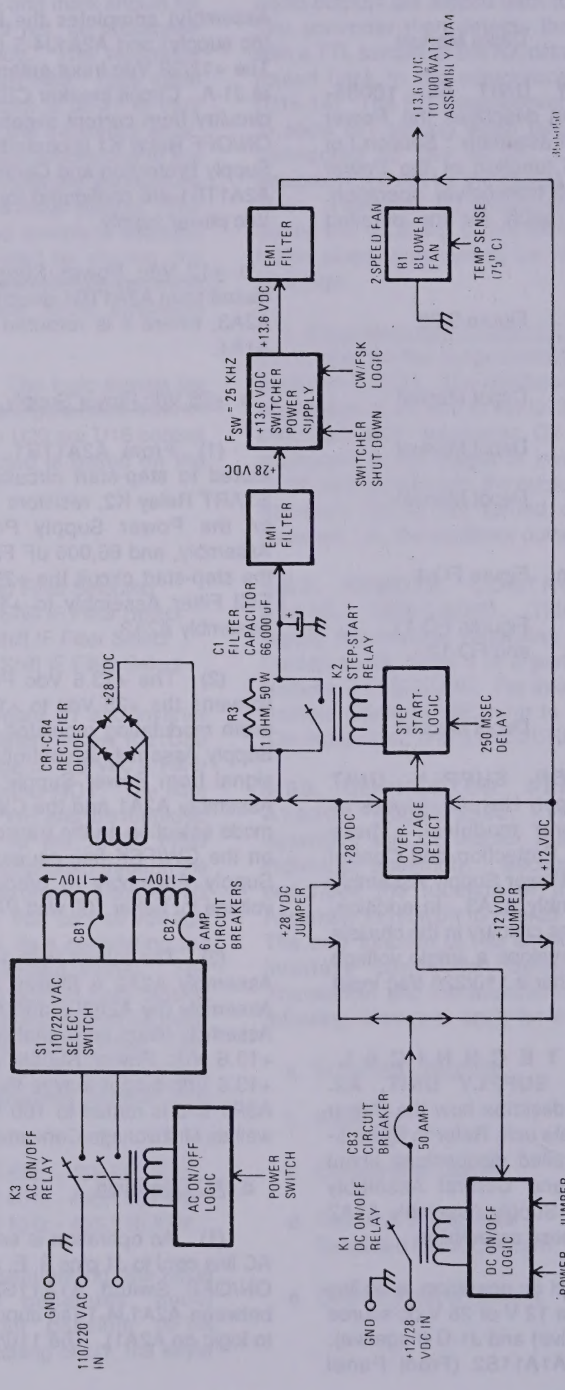


Figure 5-33. Power Supply Unit Simplified Diagram

Power Supply Unit at J1-B (hot line) and J1-E (neutral line).

(2) At the ac inputs, varistors VR1 and VR2 protect against transients greater than 275 V and clamp the input to 320 V. Following the varistors is AC ON/OFF Relay K3, which is controlled by circuitry on Power Supply Protection and Control Assembly A2A1. The configuration of 110/220 Vac Select Switch S1 determines which line voltage is correct for the primary windings of transformer T1. Circuit breakers CB1 and CB2 limit current to the transformer to 6 amperes. Lines from one of the 110 V primary windings of transformer T1 supply the 110 Vac input to the LPA/Coupler Interface Board in the 100 Watt Transceiver.

(3) Transformer T1 steps down the 110/220 Vac input to 22 Vac. The 22 Vac is then rectified to +26.5 Vdc (nominal) by rectifier diodes CR1 through CR4. The rectified signal reaches step-start circuitry and follows the same path as the +28 Vdc input signal.

(4) The Power Supply Unit houses thermistor RT1 and blower fan B1 for cooling. Besides RT1, blower fan B1 is also controlled by a digital FAN CONTROL signal from 100 Watt Assembly A1A4.

5-94. POWER SUPPLY PROTECTION AND CONTROL ASSEMBLY A2A1, 10085-0290. This manual portion describes the Power Supply Protection and Control Assembly PWB as an individual assembly. Section I of this chapter describes the function of the Power Supply Protection and Control Assembly PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. Simplified Diagram	Figure 5-34
b. Schematic Diagram	Depot Manual
c. Parts List	Depot Manual
d. Component Layout	Depot Manual
e. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
f. Overall Interconnection	Figures FO-11 and FO-12
g. Transceiver Assembly Schematic Diagrams	Depot Manual

5-95. OVERALL POWER SUPPLY PROTECTION AND CONTROL ASSEMBLY PWB FUNCTION. The Power Supply Protection and Control Assembly has seven primary functions, each of which involves circuitry on Power Supply Unit, A2:

a. Control of DC ON/OFF Relay A2K1

b. +12/+28 Vdc Configuration

c. Control of STEP-START Relay A2K2

d. Over-Voltage Protection

e. Power Supply Shut-Down Control

f. Control of Blower A2B1

g. Control of AC ON/OFF Relay A2K3

These functions are discussed in detail in the paragraphs that follow.

5-96. DETAILED PROTECTION AND CONTROL PWB CIRCUIT DESCRIPTION. Refer to simplified diagram, figure 5-34.

a. Control of DC ON/OFF Relay A2K1; Q1. When a dc power source is used and POWER ON/OFF Switch A1A11S2 on the Front Panel Assembly is in the ON position, voltage is applied to pin J1-5 of the Power Supply Protection and Control Assembly. If the voltage is of the proper polarity, diode CR1 conducts, and DC ON/OFF relay A2K1 is powered. Relay driver Q1 is enabled through R5, CR3, and CR4. As a result, DC ON/OFF Relay A2K1 on the Power Supply Unit closes, and the +12/+28 Vdc input (A2J1-A) to the Power Supply Unit reaches jumper A2JMP1. Diode CR1 protects against dc input voltage of the wrong polarity.

b. +12/+28 Vdc Configuration; A2JMP1, TB1. Jumper A2JMP1 on terminal block TB1 configures the Power Supply Protection and Control Assembly for either a +12 Vdc or a +28 Vdc power source. When A2JMP1 is configured for +12 Vdc, the +12 Vdc output at TB1-2 is connected directly to the positive supply line to the transceiver. When A2JMP1 is configured for +28 Vdc, the +28 Vdc output at TB1-1 is routed to step-start circuitry.

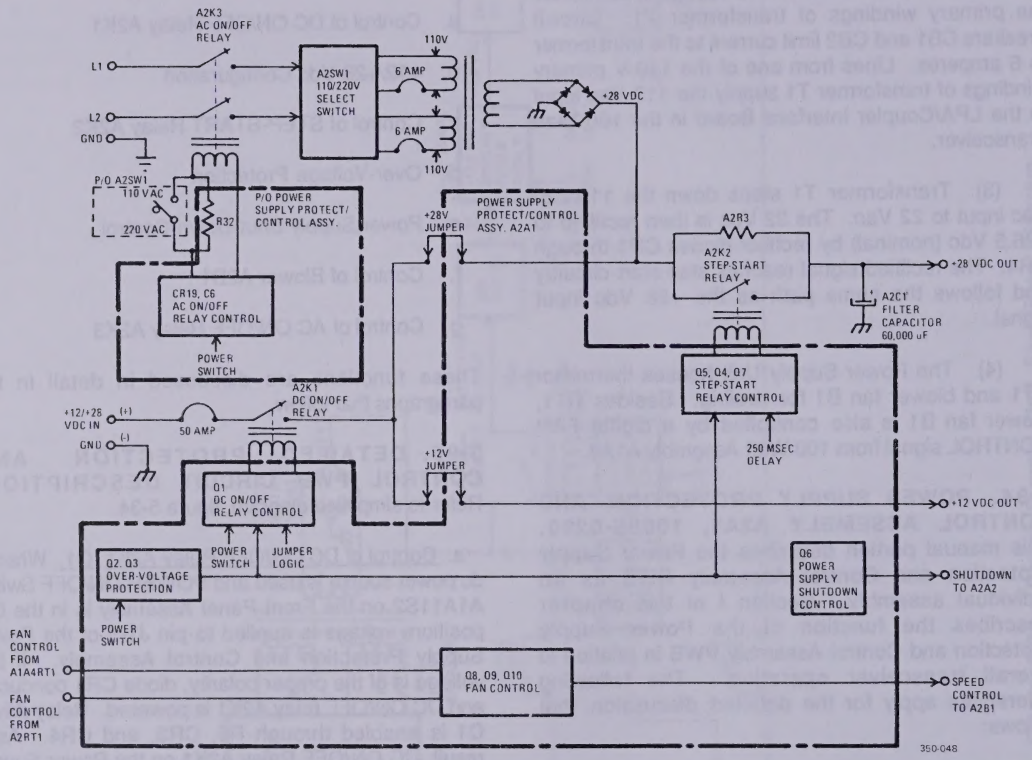


Figure 5-34. Protection and Control Assembly Simplified Diagram

c. Control of STEP-START Relay A2K2; Q5, Q4, Q7.

(1) When power (+28 Vdc) is first applied to the Power Supply, STEP-START Relay A2K2 is open. The +28 Vdc from TB1-1 is applied to 66,000 uF filter capacitor A2C1 via resistor A2R3. As A2C1 charges, capacitor C4 of the Power Supply Protection and Control Assembly charges through resistor R22. When A2C1 is approximately 80% charged, the voltage across C4 exceeds the limit of 12 V zener diode CR3 (plus the base-emitter drop), and transistor Q5 turns on. Q5 drives transistor Q4, and A2K2 closes. The delay caused by C4 is approximately 0.25 second. Reset transistor Q7 discharges C4 when the 100 Watt Transceiver is turned off, so that step-start must begin again when the 100 Watt Transceiver is turned back on.

(2) When a +12 Vdc supply is used, the step-start circuit is bypassed; however diode CR16 and resistor R28 charge up the filter capacitor so that the +13.6 Vdc Power Supply Assembly is not back-biased.

d. Over-Voltage Protection; Q2, Q3. If the source voltage is too high (over +35 Vdc with a +28 Vdc source, or over +16 Vdc when jumpered for 12 Vdc), the voltage across R9 exceeds 6.2 V (which is the drop across 5.6 V zener diode CR8 and the base/emitter of Q2). Transistor Q2 then turns on. The over-voltage detector has two resistor values for detecting excessive voltage (over 35 V or over 16 V). CR7 selects the resistor for 28 V, and diode CR6 selects the resistor for 12 V. In either case, Q2 biases transistor Q3 on, pulling down relay drivers Q1 and Q4. As a result, DC ON/OFF Relay A2K1 and STEP-START Relay A2K2 are held open.

e. Power Supply Shut-Down Control; Q6. Circuitry on the Power Supply Protection and Control Assembly also controls shut-down of +13.6 Vdc Power Supply Assembly A2A2. The SHUT-DOWN line at pin J3-3 is low (activating shut-down) when the over-voltage protection circuit is activated, when A2JMP1 is configured for a +12 Vdc supply (+13.6 Vdc Power Supply Assembly is bypassed), or during step-start delay. In each case, transistor Q4 is biased off so that transistor Q6 is biased on. Q6 pulls J3-3 to ground, which then shuts down the pulse-width modulating regulator on the +13.6 Vdc Power Supply Assembly.

f. Control of Blower A2B1; Q8, Q9, Q10.

(1) Two inputs to the Power Supply Protection and Control Assembly are used to control blower A2B1. One input is from thermistor A2RT1 on the heatsink for rectifier diodes A2CR1 through A2CR4 in the Power Supply Assembly. When the heatsink gets too hot (higher than approximately 75° C), the thermistor resistance increases, biasing transistor Q8 on. Q8 then biases on transistor Q9, which biases on transistor Q10. Q10 pulls SPEED CONTROL output pin J1-2 to ground, shorting out the voltage-limiting resistor on the fan. The fan changes from normal low speed (approximately 9 V across the fan motor) to high speed (12 V across the fan motor).

(2) The other fan control input to the Power Supply Protection and Control Assembly is a digital fan-speed command from thermistor A1A4RT1 on the 100 Watt Assembly. This signal enters the Power Supply Protection and Control Assembly at pin J4-9. When this line is low, the fan changes to high speed operation.

g. AC Operation. When POWER ON/OFF Switch A1A11S2 on the Front Panel Assembly is set to the ON position, Q14 is turned on. Anytime an ac power source is applied to the 100 Watt Transceiver, neon lamp DS1 lights. Diode CR19 rectifies the line voltage, and capacitor C6 charges, supplying 100 Vdc to the dc coil of AC ON/OFF Relay A2K3. When switch A2SW1 is configured for 110 Vac, the rectified current is fed directly into A2K3. When switch A2SW1 is configured for 220 Vac, the rectified current is routed through resistor R32. When A2K3 closes, power is applied to the primary of transformer A2T1. At the secondary of A2T1, the voltage is rectified to +28 Vdc by diodes A2CR1 through A2CR4. The +28 Vdc is then routed to step-start circuitry and follows the same path as the +28 Vdc input.

5-97. +13.6 VDC POWER SUPPLY ASSEMBLY A2A2, 10085-0260. This manual portion describes the +13.6 VDC Power Supply Assembly PWB as an individual assembly. Section I of this chapter describes the function of the +13.6 VDC Power Supply Assembly PWB in relation to overall transceiver operation. The following references apply for the detailed discussion that follows:

a. +13.6 Vdc Power Supply Overall Operation Figure 5-35

b. +13.6 Vdc Power Supply Functional Diagram	Figure 5-36
c. Simplified Regulator U1 Operation	Figure 5-37
d. Pulse Width Modulating Regulator Waveform	Figure 5-38
e. Schematic Diagram	Depot Manual
f. Parts List	Depot Manual
g. Component Layout	Depot Manual
h. 100 Watt Transceiver Simplified Block Diagram	Figure FO-1
i. Overall Interconnection	Figures FO-11 and FO-12
j. Transceiver Assembly Schematic Diagrams	Depot Manual

5-98. +13.6 VDC POWER SUPPLY ASSEMBLY OVERALL FUNCTION. Refer to figure 5-35 for this description of basic operation of the +13.6 Vdc Power Supply Assembly. The +13.6 Vdc Power Supply Assembly is a switching regulator that supplies a regulated +13.6 Vdc (at up to 40 amperes) from a supply of +18 to +33 Vdc. In basic operation, the input voltage is passed to the output filter as a train of pulses at a fixed rate. The duty cycle of the pulses is variable and is determined by the amount of error in the output voltage. Since the output filter network has a choke input, a flyback diode allows the current through the choke to continue during the off-time of the pass transistors. The pulses are integrated to yield a dc voltage at the output of the filter. This output voltage is compared to a stable reference in the regulator. The result of the comparison determines the duty cycle of the pulses and thus the output voltage.

5-99. DETAILED +13.6 VDC POWER SUPPLY CIRCUIT DESCRIPTION. For this discussion, refer to simplified diagram, figure 5-36.

a. Overall +13.6 Vdc Power Supply Assembly PWB Function. The +13.6 Vdc Power Supply Assembly develops a regulated +13.6 Vdc (or +11 Vdc in CW/FSK mode) output from a +18 to +33 Vdc input. +13.6 Vdc Power Supply Assembly A2A2 includes driver and pass transistors, an output filter, a thermal sensor, and +13.6 Vdc Power Supply PWB Assembly A2A2A1. The A2A2A1 subassembly contains a pulse-width modulating regulator, a transformer assembly, and shut-down and protection circuitry. The four major functional areas of the +13.6 Vdc Power Supply Assembly are:

1. Pulse-Width Modulating Regulator
2. Pre-Driver, Driver, and Pass Transistors
3. Transformer Assembly
4. Shut-Down Circuits

b. Pulse-Width Modulating Regulator. The Pulse-Width Modulating Regulator produces variable width output pulses at a 25 kHz rate to drive the pass transistors in the +13.6 Vdc Power Supply Assembly. The output pulse-width is proportional to the error voltage determined from the output voltage feedback input. The output voltage of the supply is proportional to the duty cycle of the pulse train and the applied input voltage.

c. Pre-Driver, Driver, and Pass Transistors. The pulse output of the pulse-width modulating regulator controls the states of the pre-driver, driver, and pass transistors. The pass transistors pass the +18 to +33 Vdc input to the output filter network (L1, C4, and C5) through the transformer assembly.

d. Transformer Assembly. The transformer assembly consists of three transformers: the driver transformer and two current-sense transformers. The driver transformer provides base drive to pass transistors Q1 and Q2 that is proportional to collector current. The current-sense transformers sense forward and flyback current, producing a current feedback signal that is input to the pulse-width modulating regulator via a filter network.

e. Shut-Down Circuits. There are four interconnecting shut-down circuits. They are over-temperature shut-down, step-start (external) shut-down, under-voltage shut-down, and over-voltage shut-down. When any of these circuits is activated, the pulse-width modulating regulator is shut down by reducing the duty cycle of its output to 0%. As a result, the +13.6 Vdc output of the +13.6 Vdc Power Supply Assembly is switched off.

f. Detailed +13.6 Vdc Power Supply Assembly Circuit. The paragraphs below are dedicated to

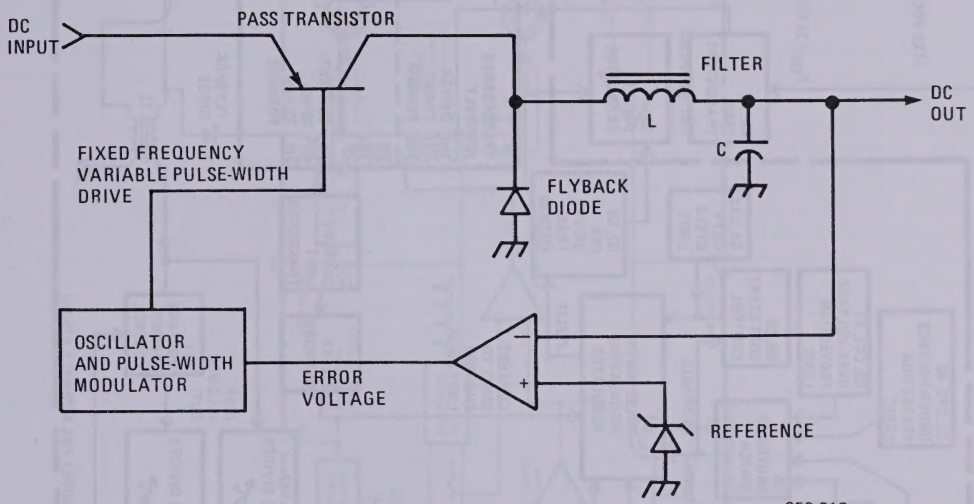


Figure 5-35. +13.6 Vdc Power Supply Overall Operation

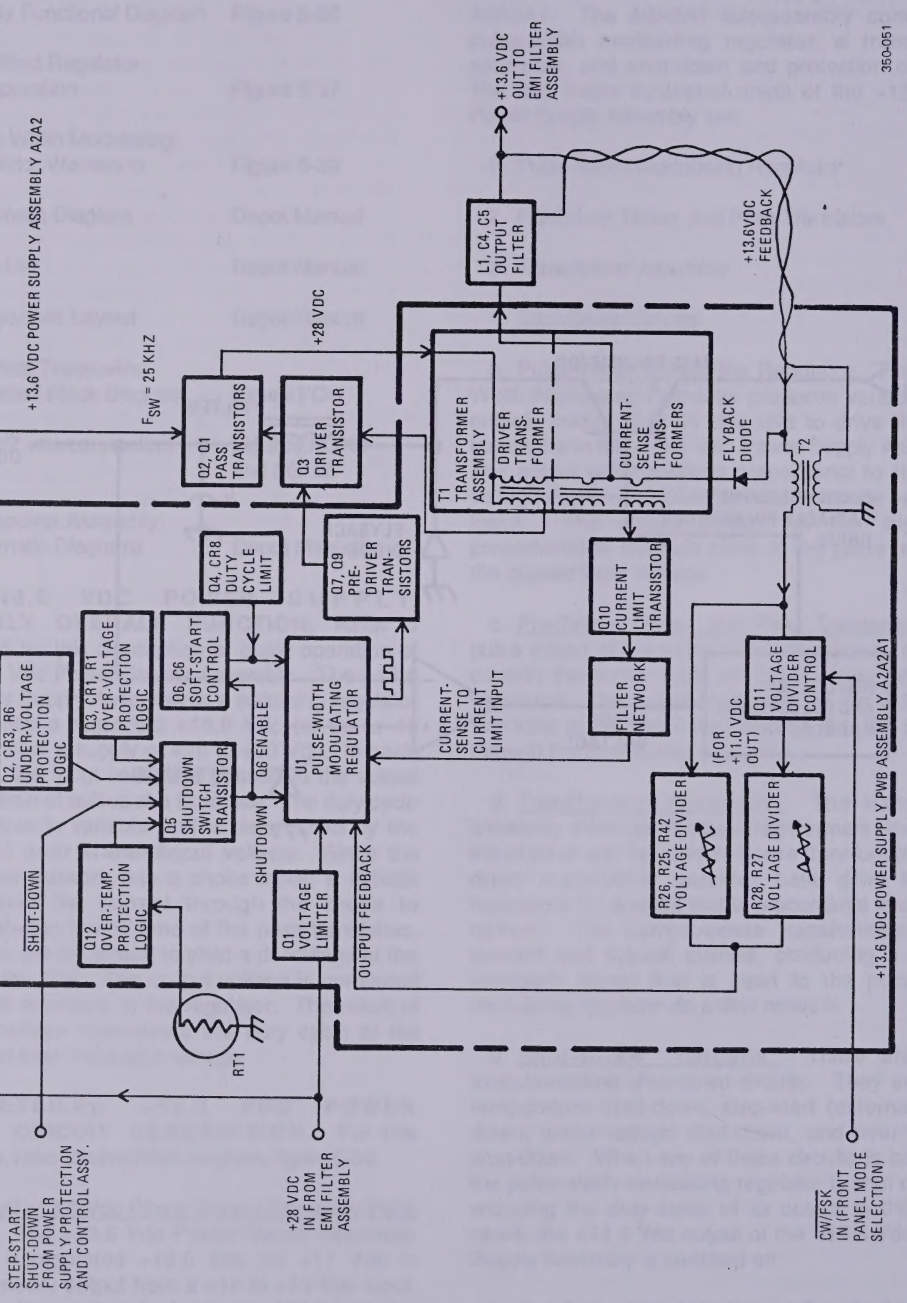


Figure 5-36. +13.6 Vdc Power Supply Functional Diagram

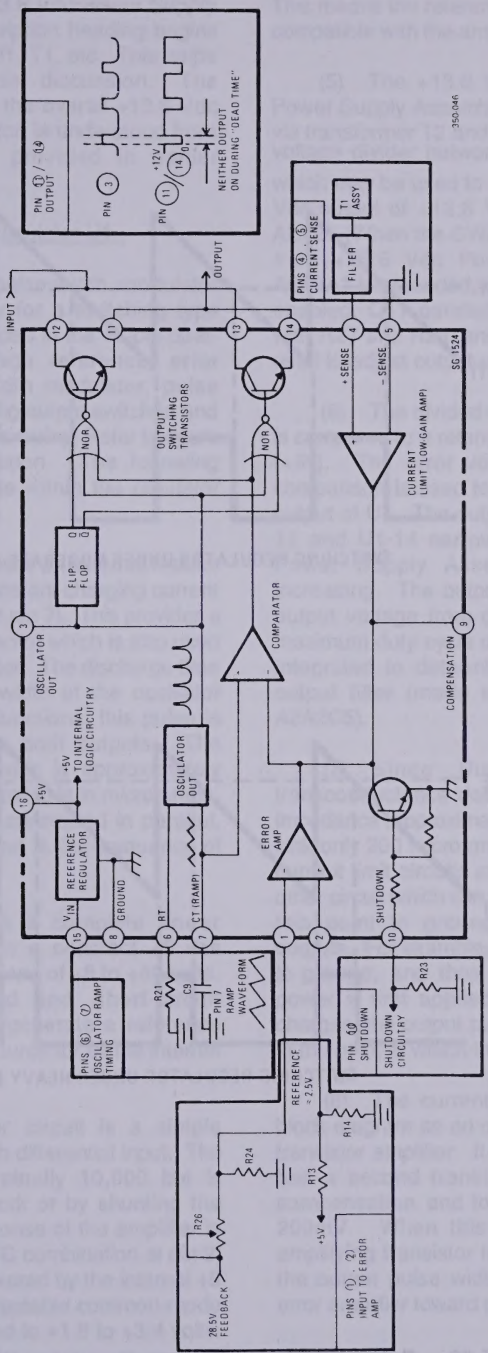


Figure 5-37. Simplified Regulator U1 Operation

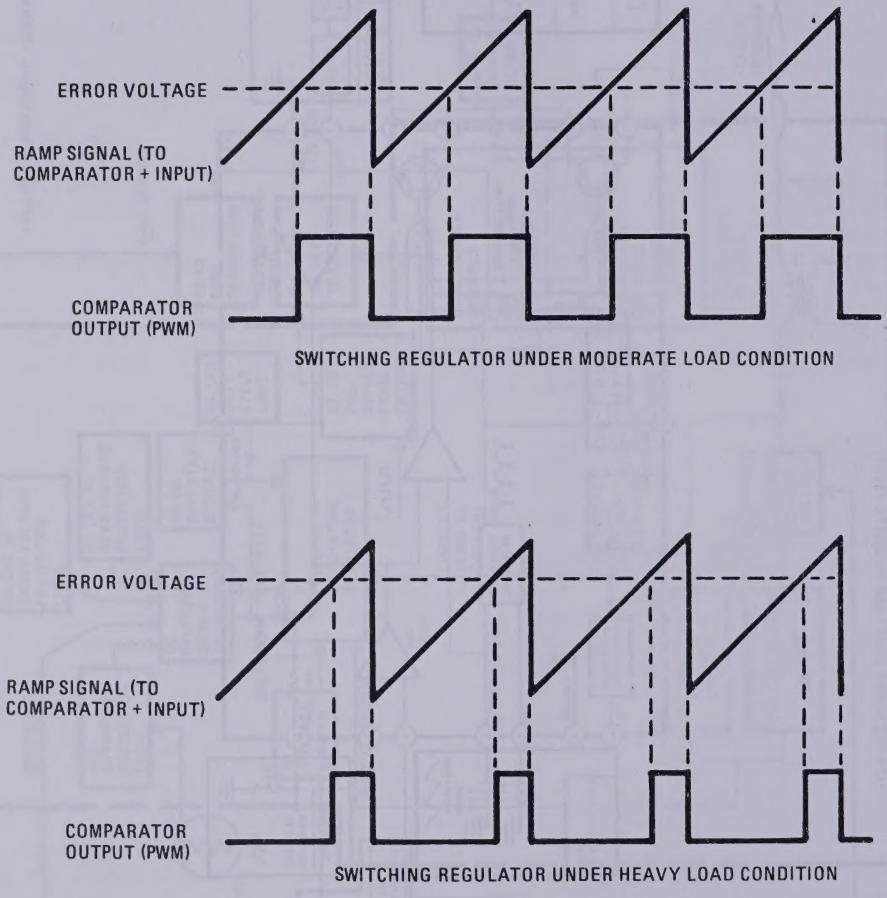


Figure 5-38. Pulse Width Modulating Regulator Waveform

detailed descriptions of the +13.6 Vdc Power Supply Assembly circuits. Each description heading begins with a device number, e. g. , U1, T1, etc. This helps identify the exact circuit under discussion. The detailed information assumes the overall +13.6 Vdc Power Supply Assembly function is understood from the simplified descriptions provided in earlier paragraphs.

g. Pulse-Width Modulating Regulator U1.

(1) U1 is a regulating pulse-width modulator containing all control circuitry for a switching type regulated power supply. Included in the 16-pin dual-in-line package is the voltage reference, error amplifier, oscillator, pulse-width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. Refer to figure 5-37 for simplified U1 operation. The following discussion describes elements within the regulator chip.

(2) The oscillator in U1 uses an external resistor (R21 at pin 6) to establish a constant charging current into an external capacitor (C9 at pin 7). This provides a linear ramp voltage on the capacitor which is also used as a reference for the comparator. The discharge time of C9 determines the pulse width of the oscillator output pulse. Among other functions, this pulse is used as a blanking pulse to both outputs. The oscillator period in micoseconds is approximately t=(0.8)RC where R is in ohms and C is in microfarads. The two switcher outputs are connected in parallel, and the frequency of the output is the frequency of the oscillator.

(3) Within U1, there is a complete linear regulator designed to provide a constant +5 volt output with input voltage variations of +8 to +40 volts. It is internally compensated and short-circuit protected. It is used both to generate a reference voltage and as the regulated source for all the internal timing and controlling circuitry.

(4) The error amplifier circuit is a simple transconductance amplifier with differential input. The gain of this amplifier is nominally 10,000 but is reduced by a feedback network or by shunting the output to ground. Phase response of the amplifier is compensated by an external RC combination at pin 9. Since the error amplifier is powered by the internal +5 volt reference voltage, the acceptable common-mode input voltage range is restricted to +1.8 to +3.4 volts. This means the reference must be divided down to be compatible with the amplifier input.

(5) The +13.6 Vdc output of the +13.6 Vdc Power Supply Assembly is fed back to pin U1-1 (-IN) via transformer T2 and a voltage-divider network. The voltage divider network includes V_{Out} Adjust R26, which may be used to adjust the voltage at the +13.6 Vdc output of +13.6 Vdc Power Supply Assembly A2A2. (When the CW/FSK mode is selected, pin J1-1 on +13.6 Vdc Power Supply PWB Assembly A2A2A1 is grounded, enabling transistor Q11. When enabled, Q11 parallels the voltage divider network with R27 and R28, and CW/FSK Adjust R28 may be used to adjust output voltage.)

(6) The divided-down feedback voltage at U1-1 is compared to a reference voltage (2.5 V) at pin U1-2 (+IN). The error voltage that results from this comparison is used to control the pulse-width at the output of U1. The output pulse at the junction of U1-11 and U1-14 narrows to prevent the +13.6 Vdc Power Supply Assembly output voltage from increasing. The output pulse widens to prevent the output voltage from decreasing. The signal has a maximum duty cycle of 80%. The output pulses are integrated to determine the dc component in the output filter (made up of A2A2L1, A2A2C4, and A2A2C5).

(7) Since the error amplifier is a transconductance design, the output is a very high impedance (approximately 5M ohm) and can source or sink only 200 microamperes. Internal shut-down and current limit circuits are connected at pin 9, but any other circuit which can sink 200 microamperes can pull this point to ground, thereby shutting off both outputs. For example, the soft start circuit holds pin 9 to ground, and thus holds both outputs off when power is first applied. As the soft-start capacitor charges, the output pulse slowly increases from zero to the point at which the feedback loop takes control.

(8) The current limiting circuit, shown in the block diagram as an operational amplifier, is a single transistor amplifier. It is frequency compensated and has a second transistor to provide temperature compensation and to reduce the input threshold to 200mV. When this threshold is exceeded, the amplifying transistor turns on and linearly decreases the output pulse width by pulling the output of the error amplifier toward ground.

(9) The outputs of U1 are two identical NPN transistors with both collectors and emitters routed to output pins. These circuits include an antisaturation network for fast response and current limiting set for a maximum output current of approximately 100 mA.

(10) The +18 to +33 Vdc input to +13.6 Vdc Power Supply Assembly A2A2 is routed via transistor Q1 (A2A2A1Q1) to pins U1-12 (CA) and U1-13 (CB) of the pulse-width modulating regulator. The voltage at these pins is routed via two internal transistors (when enabled) to output pins U1-11 (EA) and U1-14 (EB).

(11) The operation of the pulse-width modulating regulator is shown in figure 5-38. The Pulse Width Modulation (PWM) duty cycle varies with line voltage and varies slightly with load. This in turn will vary the on-time of the pass transistors to give the exact pulse-width needed to produce the desired output voltage. The output is then filtered to provide a regulated voltage with little ripple content and good regulation.

h. Pre-Driver, Driver, and Pass Transistors Q7, Q9, Q3, Q1, and Q2. Pre-Driver Transistors Q7 and Q9 translate the +5 V pulse output from pins U1-11 and U1-14 up to the logic level needed to drive transistor Q3. (Approximately 0.2 to 0.3 amperes are needed to drive Q3.) Pass transistors Q1 and Q2 switch on and off at a 25 kHz rate, passing the pulse-width modulated dc input to the output filter.

i. Transformer Assembly T1.

(1) Transformer Assembly T1 consists of two current-sense transformers and a driver transformer. The outputs from the secondaries of the current-sense transformers are rectified by diodes CR10 and CR11 and then passed through Q10 to a filter network. The filter network provides phase compensation to achieve the proper loop response at current sense input pin U1-4 (CL+).

(2) When the voltage at pin U1-4 exceeds the threshold of 700 mV, control of the +13.6 Vdc regulator is taken over by the current limit network. The output current is held constant, while the output voltage is allowed to drop.

(3) The driver transformer of Transformer Assembly T1 is a current transformer with a 1:10 turns ratio. The primary of the driver transformer samples the collector current in the pass transistors and provides a base current that is inversely proportional to the turns ratio. Thus, base current equals one tenth of the collector current.

j. Shut-Down/Soft-start Q5, Q6. When any of the shut-down circuits (Over-Temperature, Step-Start, Under-Voltage, or Over-Voltage) is activated, transistor Q5 is biased on. A high appears on pin U1-10 (S/D), which shuts down Pulse-Width Modulating Regulator U1. In addition, transistor Q6 is enabled so that soft-start capacitor C6 is discharged through resistor R19. When U1 is enabled again, C6 charges (by 200 uA supplied at pin U1-9) to bring the duty cycle of U1 up slowly.

k. Over-Temperature Shut-Down Q12. If thermistor RT1 (A2A2RT1) senses a temperature above approximately 75 degrees centigrade, it biases on transistor Q12. When enabled, Q12 causes transistor Q5 to bias on, and Pulse-Width Modulating Regulator U1 is shut down.

l. Step-Start Shut-Down Circuit (Activated Externally). Pulse-Width Modulating Regulator U1 is shut down while the 60,000 uF filter capacitor in the step-start circuit on the Power Supply Protection and Control Assembly charges. A low on the line from the Power Supply Protection and Control Assembly to input pin J1-6 on +13.6 Vdc Power Supply PWB Assembly A2A2A1 initiates this shut-down. Pin J1-6 is tied to the collector of transistor Q12 (used in the over-temperature shut-down circuit). Step-start shut-down uses the same shut-down circuit as over-temperature shut-down.

m. Voltage Limiter Q1 (A2A2A1Q1).

(1) At normal line voltages, transistor Q1 acts as an emitter-follower, passing the input from the EMI Filter Assembly to pulse-width modulating regulator inputs U1-12 (CA), U1-13 (CB), and U1-15 (VCC), as well as to shut-down circuitry.

(2) Q1 also acts as a voltage-limiter to protect U1 against spikes in the line voltage. Q1 limits the voltage at its emitter to approximately 27 V, referenced at zener diode CR1.

n. Under-Voltage Shut-down Q2, CR3, R6. Until the line voltage rises to approximately +17 V, transistor Q2 is biased off and transistor Q5 is biased on so that Pulse-Width Modulating Regulator U1 is disabled. When the line voltage reaches approximately +17 V, zener diode CR3 breaks down

and current flows through resistor R3 so that transistor Q2 is biased on. The base of Q5 is pulled above +5 V so that Q5 is off, enabling Pulse-Width Modulating Regulator U1.

o. Over-Voltage Shut-Down Q3, CR1, R1. At excessive voltages (above approximately 35 V), diode CR1 breaks down, and current flows through resistor R10, enabling transistor Q3. The enabled Q3 grounds the junction of R7 and R8, pulling the base of Q5 below 5 V. Q5 turns on, causing the shut-down of Pulse-Width Modulating Regulator U1.

p. Duty Cycle Limit Q4, CR8. Transistor Q4 limits the error voltage, and thus the duty cycle, of U1 to approximately 80%. Q4 accomplishes this limiting by controlling the maximum voltage level at compensation input pin U1-9 (COMP) through diode CR8.

5-100. EMI FILTER ASSEMBLY, A2A3, 10085-0240. The EMI Filter Assembly, shown in figure 5-33, filters any spurious signals from the input and the output of +13.6 Vdc Power Supply PWB Assembly A2A2. The +13.6 Vdc output from the EMI Filter Assembly is routed to the Multivoltage Supply Assembly and the 100 Watt Power Amplifier in the 100 Watt Transceiver. The EMI Filter Assembly is a sealed unit and does not contain serviceable components.

CHAPTER 6

MAINTENANCE

WARNING

Dangerous voltages exist in this radio equipment. Before removing any covers, disconnect the primary power.

Section I. INTRODUCTION

6-1. CHAPTER ORGANIZATION. This chapter is divided into five sections. Section I tells how the chapter is organized, describes the on-equipment maintenance philosophy, and introduces you to the concept of BIT (Built-In Test). Section II is a detailed presentation of how to use BIT to troubleshoot and repair the 100 Watt Transceiver. Section III consists of removal and replacement procedures for the faulty modules identified by BIT. Section IV is dedicated to Periodic Maintenance Procedures. Section V contains alignment procedures for the replaceable modules.

6-2. ON-EQUIPMENT MAINTENANCE PHILOSOPHY. The 100 Watt Transceiver is designed so that you can make most repairs without removing the equipment from its location. The procedures in this chapter should enable you to identify and correct most equipment malfunctions within 15 minutes.

NOTE

Field and Organizational Maintenance of the modules and circuit card assemblies is limited only to the removal, replacement, and alignments given in chapter 6.

Tool List

Screwdrivers:

3/16-inch flat blade (4 inches long)
No. 1 Phillips
No. 2 Phillips
Phillips, right-angle, ratchet (optional)

Wrenches:

6-inch adjustable
0.050-inch Allen

Nut Drivers:

3/16, 9/16, 1/4, 5/16 (optional)

Needle Nose Pliers (optional)

Alignment Tool Kit

6-3. BIT (BUILT-IN TEST). The key to servicing the 100 Watt Transceiver is a feature called BIT. BIT, which is an acronym for Built-In Test, consists of several systems, some manual and some automatic. These systems are the front panel controls and displays (including a multi-function meter), periodic automatic status checking, a manual diagnostic routine, and automatic diagnostic routines (one for receive only and one for transmit and receive). When used in conjunction with this manual, these systems allow rapid and accurate fault diagnosis.

NOTE

The BIT is designed to only catch malfunctions of the major subassemblies/modules of the Radio System. Multiple fault anamolies may not be discriminated properly by the BIT. Also the BIT can generate random misdiagnosis of modules, due to vagaries such as contact bounce in relays or high RF noise near the radio. Any BIT indictment of modules should be repeated 3 times in a row to ensure proper diagnosis.

Section II. PERFORMANCE TESTING AND TROUBLE ANALYSIS USING BIT

6-4. FRONT PANEL CONTROLS AND DISPLAYS. The front panel controls and displays are utilized to control and monitor equipment operation during fault diagnosis. The displays provide an indication of equipment status, and a built-in meter allows analog monitoring of the parameters listed in Table 6-1. See Chapter 4 in this manual for a detailed discussion of all the controls and indicators.

6-5. PERIODIC AUTOMATIC STATUS CHECKING. The equipment performs periodic status checks on itself whenever it is energized. These checks are performed automatically and require no interaction or commands from the operator. These checks include the following and result in the indications or actions listed:

CHECK	RESULT
Synthesizer lock	The FAULT light comes on if the synthesizer is out of lock
Reference/BFO lock	The FAULT light comes on if the BFO is out of lock
Keying status	The XMIT indicator comes on when the transceiver is keyed
Low output power when transceiver is keyed	The LO PWR indicator comes on
Basic microprocessor operation	Automatic microprocessor reset* when a malfunction occurs
13.6 V supply level	The microprocessor is held in the reset* condition if the supply voltage is low

* The reset condition is characterized by a "frozen" display; in other words, the display remains exactly as it was when the reset occurred. None of the front panel controls has any effect on it.

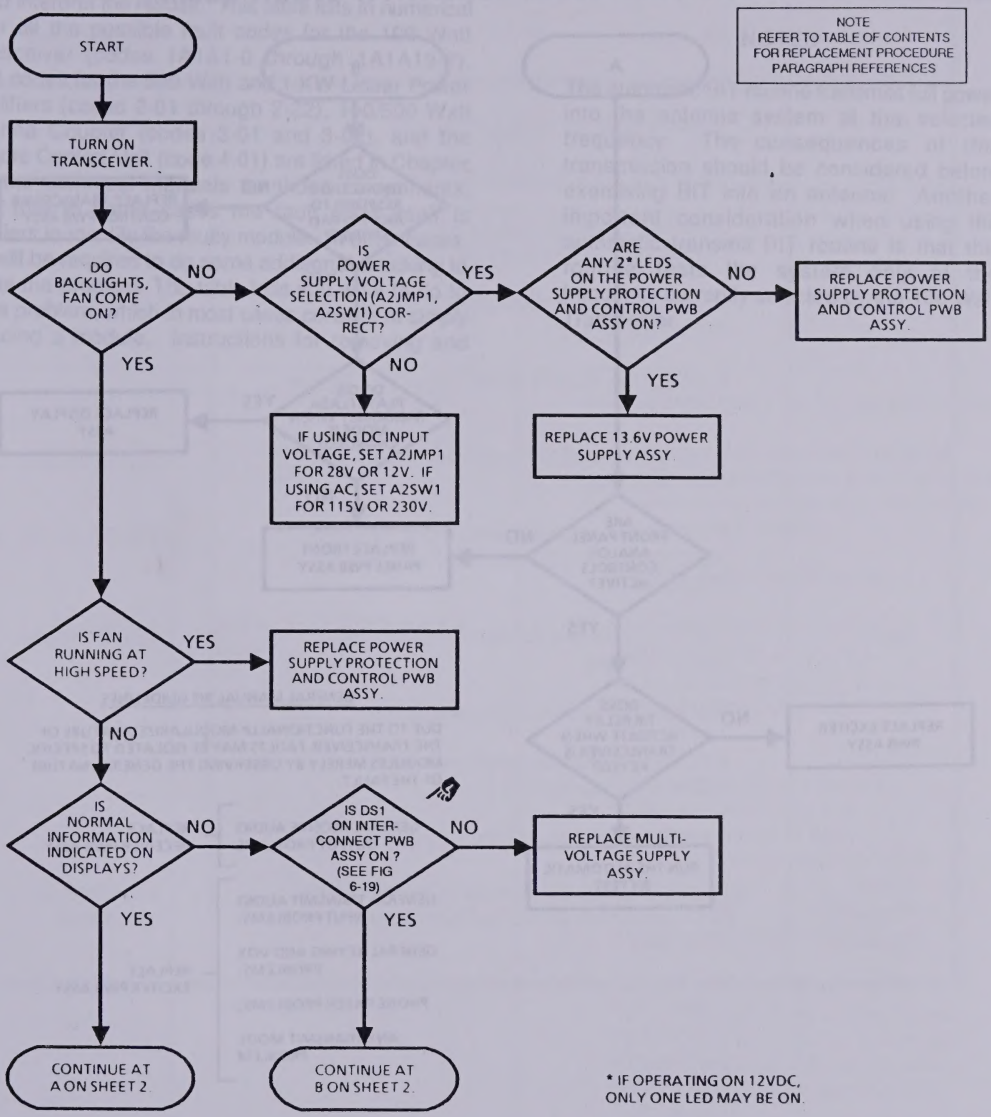
6-6. MANUAL DIAGNOSTIC BIT ROUTINE. A manual BIT routine is included in this section to assist in fault diagnosis. Figure 6-1, which is a flowchart of the steps in this routine, provides a sequence of observations which can be used to supplement the automatic BIT routines described in the following paragraph.

6-7. AUTOMATIC DIAGNOSTIC BIT ROUTINES. The automatic BIT routines are used to test the operation of the 100 Watt Transceiver. These BIT routines operate in the same manner as a skilled technician, first checking the operation or outputs of key modules such as the microprocessor, power supply, and synthesizer and then signal-tracing the main receive and transmit signal paths from input to output, varying key parameters such as band or mode as the test proceeds. Upon detection of a fault, the process stops and the corresponding fault code is displayed. The Appendix at the end of this chapter indicates the sequence of events that occurs during the automatic BIT routines. The receive-only routine includes steps 1-14, whereas the transmit/receive routine encompasses all 22 steps. Successful completion of these routines assures you that the transceiver is operationally ready for use. Running the automatic diagnostic BIT routines for performance testing and verification is therefore another major use of this feature.

6-8. TROUBLESHOOTING WITH BIT. The first stage in the troubleshooting process is becoming aware that a fault condition exists. This usually happens as the result of an observation (for example, you notice that the FAULT light is on) or as the result of a deterioration in the equipment's performance (for example, the person you're communicating with informs you that your signal is very weak). In any case, it's always a good idea to make a note whenever you notice anything unusual. This will come in handy if you have to do any troubleshooting. The nature of the fault determines whether you should use the manual BIT routine or the automatic BIT routines.

a. Using the Manual BIT Flowchart. The manual BIT flowchart, Figure 6-1, is used when the 100 Watt Transceiver is powered up and there is an obvious problem or symptom observed. It suggests preliminary observations and actions that you should perform before you initiate an automatic BIT routine. Sometimes, when there is a problem with the display or the keypad is inoperative, you cannot use the automatic BIT routines at all. In these cases, you must rely entirely on the manual BIT flowchart.

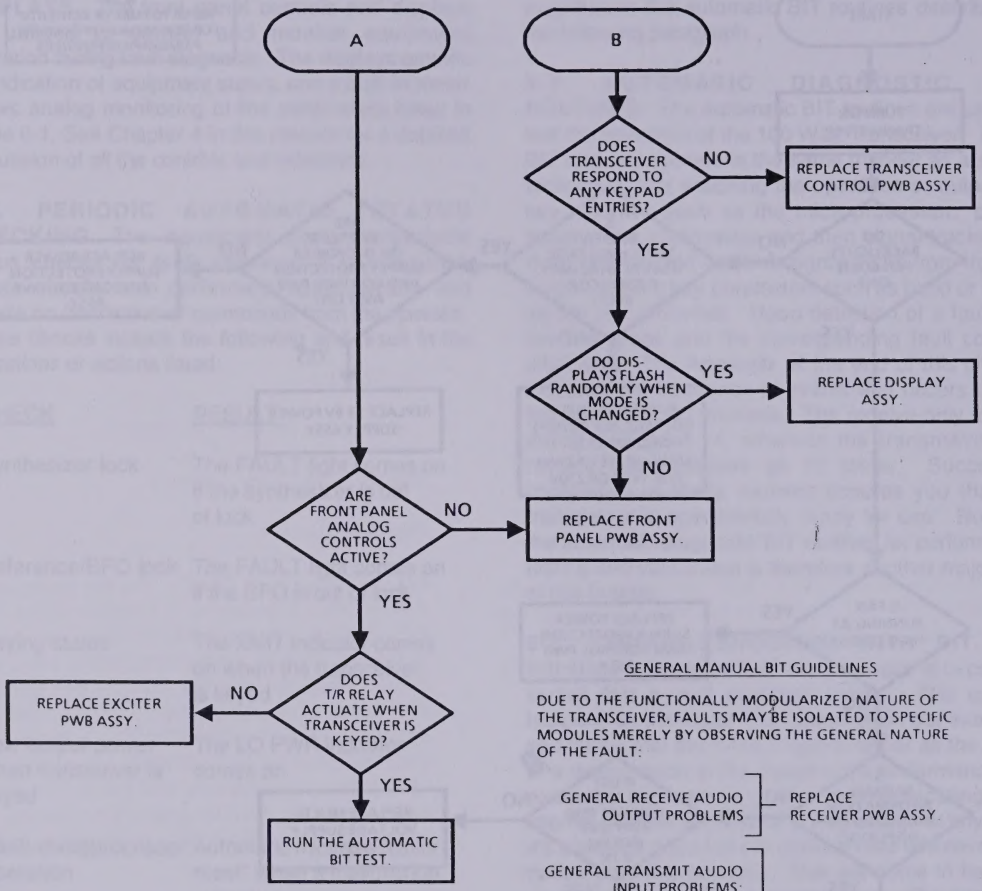
MANUAL BIT FAULT ISOLATION CHART


START
TURN ON TRANSCEIVER.
DO BACKLIGHTS, FAN COME ON?
NO
YES
IS POWER SUPPLY VOLTAGE SELECTION (A2JMP1, A2SW1) CORRECT?
YES
NO
IF USING DC INPUT VOLTAGE, SET A2JMP1 FOR 28V OR 12V. IF USING AC, SET A2SW1 FOR 115V OR 230V.
ARE ANY 2* LEDS ON THE POWER SUPPLY PROTECTION AND CONTROL PWB ASSY ON?
NO
YES
REPLACE POWER SUPPLY PROTECTION AND CONTROL PWB ASSY.
REPLACE 13.6V POWER SUPPLY ASSY.
NOTE
REFER TO TABLE OF CONTENTS FOR REPLACEMENT PROCEDURE PARAGRAPH REFERENCES
IS FAN RUNNING AT HIGH SPEED?
YES
NO
REPLACE POWER SUPPLY PROTECTION AND CONTROL PWB ASSY.
IS NORMAL INFORMATION INDICATED ON DISPLAYS?
NO
YES
IS DS1 ON INTER-CONNECT PWB ASSY ON ? (SEE FIG 6-19)
NO
YES
REPLACE MULTI-VOLTAGE SUPPLY ASSY.
CONTINUE AT A ON SHEET 2.
CONTINUE AT B ON SHEET 2.
* IF OPERATING ON 12VDC, ONLY ONE LED MAY BE ON.

*350-067-1

Figure 6-1. Manual BIT Fault Isolation Chart (Sheet 1 of 2)

MANUAL BIT FAULT ISOLATION CHART (Cont.)


A
B
DOES TRANSCEIVER RESPOND TO ANY KEYPAD ENTRIES?
NO
REPLACE TRANSCEIVER CONTROL PWB ASSY.
YES
DO DIS-PLAYS FLASH RANDOMLY WHEN MODE IS CHANGED?
YES
REPLACE DISPLAY ASSY.
NO
ARE FRONT PANEL ANALOG CONTROLS ACTIVE?
NO
REPLACE FRONT PANEL PWB ASSY.
YES
DOES T/R RELAY ACTUATE WHEN TRANSCEIVER IS KEYED?
NO
REPLACE EXCITER PWB ASSY.
YES
RUN THE AUTOMATIC BIT TEST.
GENERAL MANUAL BIT GUIDELINES
DUE TO THE FUNCTIONALLY MODULARIZED NATURE OF THE TRANSCEIVER, FAULTS MAY BE ISOLATED TO SPECIFIC MODULES MERELY BY OBSERVING THE GENERAL NATURE OF THE FAULT:
GENERAL RECEIVE AUDIO OUTPUT PROBLEMS
REPLACE RECEIVER PWB ASSY.
GENERAL TRANSMIT AUDIO INPUT PROBLEMS;
GENERAL KEYING AND VOX PROBLEMS;
PHONE PATCH PROBLEMS;
ANY TRANSMIT MODE PROBLEM
REPLACE EXCITER PWB ASSY.

*350-067-2

Figure 6-1. Manual BIT Fault Isolation Chart (Sheet 2 of 2)

b. Using the Automatic BIT Routines. When you initiate an automatic BIT routine, you must use Table 6-2 to interpret the results. This table lists in numerical order all the possible fault codes for the 100 Watt Transceiver (codes 1A1A1-0 through 1A1A19-2). Fault codes for the 500 Watt and 1 KW Linear Power Amplifiers (codes 2-01 through 2-22), 100/500 Watt Antenna Coupler (codes 3-01 and 3-02), and the Remote Control Unit (code 4-01) are listed in Chapter 6 of the technical manuals for those components. Note that in some cases the fault code itself is sufficient to identify the faulty module. In other cases, you will be required to do some additional checking to isolate the problem. The table tells you what to do to fix the problem, which in most cases consists of simply replacing a module. Instructions for removing and replacing the modules can be found in Section III of this chapter, "Removal/Replacement Procedures."

NOTES

The automatic BIT routine transmits full power into the antenna system at the selected frequency. The consequences of this transmission should be considered before exercising BIT into an antenna. Another important consideration when using the automatic transmit BIT routine is that this routine tests the system only at the frequency currently selected by the 100 Watt Transceiver.

Table 6-1. Meter Functions

Function	Parameter	Range/Units
AUDIO	Transmit audio on Exciter PWB Assy	-20 to +10 dB
LINE	Receive audio at output of Receiver PWB Assy	-20 to +10 dBm
	In REMOTE operation and if KEYED, line audio into Exciter PWB Assy will be monitored	
PATCH	If KEYED, transmit audio input to Exciter PWB Assy	-20 to +10 dBm
	If UNKEYED, receive audio output from Exciter PWB Assy	
FWD	If KEYED, forward RF output from Low Pass Filter PWB Assy	0 to 150 Watts
	If UNKEYED, relative receive signal strength (AGC Voltage) from AGC/TGC PWB Assy will be monitored	S3 to S9+60 dB
REF	If KEYED, reflected RF power at Low Pass Filter PWB Assy	0 to 150 Watts
	If UNKEYED, relative signal strength	
VSWR	If KEYED, VSWR computed from FWD and REF measurements	1 to 4
	If UNKEYED, relative signal strength	
AFSK (if option installed)	Average received frequency relative to center tuned frequency at AFSK Keyer/Converter PWB Assy	± the mark-to-space shift

Table 6-2. Fault Code Chart

NOTE

Refer to Table of Contents for replacement procedure paragraph references.

NOTE

This table lists only the fault codes for the 100 Watt Transceiver (codes 1A1A1-0 through 1A1A19-2). For an explanation of the fault codes for the LPA (Linear Power Amplifier, codes 2-01 through 2-22), the 100/500 Watt Antenna Coupler (codes 3-01 and 3-02), and the Remote Control Unit (code 4-01), refer to Chapter 6 of the technical manuals for those equipments.

Code	Explanation	Procedure
1A1A1-0	NO EXCITER MODULE	Install and/or connect the Exciter PWB Assy.
1A1A1-1 *	NO 455 KHZ MODULATOR OUTPUT.	a. If the meter indicates that the carrier is not present with the transceiver keyed in AME mode, replace the LPA/Coupler interface PWB Assy. b. Replace the Exciter PWB Assy.
1A1A1-2 *	NO 40 MHZ MODULATOR USB	a. If the PPC (DS1) light on the AGC/TGC PWB Assy is on during frequency and mode changes, replace the AGC/TGC PWB Assy. b. If the meter indicates that the carrier is present with the transceiver keyed in AME mode, replace the Receiver PWB Assy. c. Replace the Exciter PWB Assy.
1A1A1-3	NO 40 MHZ MODULATOR AME OUTPUT.	a. If the ribbon cable on the AGC/TGC PWB Assy is disconnected and the RFIN meter on the LPA indicates output power from the transceiver in CW mode, replace the AGC/TGC PWB Assy. b. Replace the Exciter PWB Assy.

* This fault code may be caused by the MIC potentiometer on the transceiver front panel being set too low. Before replacing any of the modules, try turning the potentiometer clockwise. Then run the transmit-receive BIT test again to see if this corrects the problem.

Table 6-2. Fault Code Chart
(continued)

Code	Explanation	Procedure
1A1A1-4	NO 40 MHZ MODULATOR CW OUTPUT.	Replace the Exciter PWB Assy.
1A1A2-1	NO USB IF.	Replace the Filter PWB Assy.
1A1A2-2	NO LSB IF.	Replace the IF Filter PWB Assy.
1A1A2-3	NO CW IF.	Replace the IF Filter PWB Assy.
1A1A3-1	NO FIRST CONVERTER RX.	Replace the First Converter PWB Assy.
1A1A3-2	NO FIRST CONVERTER TX.	a. If the PPC (DS1) light on the AGC/TGC PWB Assy is always on and the meter indicates approximately 4 W of output power in CW mode, replace the AGC/TGC PWB Assy. b. Replace the First Converter PWB Assy.
1A1A4-1	NO PA OUTPUT.	a. If the forward power output of the transceiver is approximately 8.4 W, replace the First Converter PWB Assy. b. Replace the Power Amplifier Assy.
1A1A4-2	REMOTE CONTROL MODULE.	a. Remove and replace remote control interface PWB.
1A1A5-1 -2 -3 -4 -5 -6 -7	LPF BAND 1 OPEN (RX). LPF BAND 2 OPEN (RX). LPF BAND 3 OPEN (RX). LPF BAND 4 OPEN (RX). LPF BAND 5 OPEN (RX). LPF BAND 6 OPEN (RX). LPF LATCHED CLOSED.	Replace the Low Pass Filter PWB Assy.
1A1A5-8	VSWR FAULT.	Check the connections between the transceiver and the LPA, the LPA and the antenna coupler, and the antenna coupler and the antenna.

Table 6-2. Fault Code Chart
(continued)

Code	Explanation	Procedure
1A1A5-9	TX LPF OPEN.	a. If no forward power is indicated on the meter, replace the AGC/TGC PWB Assy. b. Replace the Low Pass Filter PWB Assy.
1A1A6-1	HIGH AGC.	If Fault Code 1A1A6-1 appears with antenna connected, remove power, then remove antenna connection, attach dummy load. If Fault Code reappears replace the AGC/TGC PWB Assy.
1A1A6-2	NO MANUAL RF GAIN CONTROL	a. If the AGC voltage can be adjusted with the RF GAIN control, replace the Receiver PWB Assy. b. Replace the AGC/TGC PWB Assy.
1A1A6-3	TGC SET POINT BAD.	Replace the AGC/TGC PWB Assy.
1A1A6-4	NO TGC.	a. If the PPC (DS1) light on the AGC/TGC PWB Assy is on whenever the transceiver is keyed in CW mode, replace the Exciter PWB Assy. b. Replace the Power Amplifier Assy in any of the following situations: (1) Code 1A1A6-4 is displayed when BIT test is run at 1.6 MHz, but changes to a 1A1A4-1 at 29.9 MHz. (2) Code 1A1A6-4 is displayed when the BIT test is run at 29.9 MHz, but changes to 1A1A4-1 at 1.6 MHz. (3) The meter indicates approximately 50 W of forward power at 1.6 and 29.9 MHz. c. Replace the AGC/TGC PWB Assy.

Table 6-2. Fault Code Chart
(continued)

Code	Explanation	Procedure
1A1A7-0	NO RECEIVER MODULE.	Install and/or connect the Receiver PWB Assy.
1A1A7-1	NO 2ND CONVERTER RX SIGNAL	a. If the S meter indicates S9+40 dB with the RF GAIN control set to the maximum, replace the First Converter PWB Assy. b. After power on, if there is no receive function until MODE is scrolled, replace the Reference/BFO PWB Assy. c. Replace the Receiver PWB Assy.

Table 6-2. Fault Code Chart (continued)

Code	Explanation	Procedure
1A1A7-2*	LOW LINE LEVEL.	Replace the Receiver PWB Assy.
1A1A7-3	BAD RECEIVER T/R SWITCH (NO TX SIGNAL).	Replace the Receiver PWB Assy.
1A1A7-4	AGC SET POINT BAD.	a. If the receive signal strength meter does not respond to any signal and if strong signals sound distorted, replace the AGC/TGC PWB Assy. b. Replace the Receiver PWB Assy.
1A1A8	Not used.	
1A1A9-1	BFO UNLOCK.	Replace the Reference/BFO PWB Assy.
1A1A10-0	NO SYNTHESIZER MODULE.	Install and/or connect the Synthesizer PWB Assy.
1A1A10-1	SYNTHESIZER UNLOCK	a. If there is no background noise in AME mode and if there is no change in the background noise with the reference oscillator cable (at J2) on the Reference /BFO PWB Assy disconnected, replace the Crystal Oscillator Assy. b. Replace the Synthesizer PWB Assy.
1A1A11	Not used.	
1A1A12-1	A/D CONVERTER DEFECT	Replace the Transceiver Control PWB Assy.
1A1A13-0	NO LPA/COUPLER INTERFACE PWB ASSY.	Install and/or connect the LPA/Coupler Interface PWB Assy.
1A1A14-1 -2	HIGH MULTIVOLTAGE SUPPLY LOW MULTIVOLTAGE SUPPLY	Replace the Multivoltage Supply Assy.
1A1A15	Not used.	

*The line level may be unusually low because of the setting of the LINE potentiometer on the transceiver front panel. Before replacing the Receiver PWB Assy, try turning this potentiometer clockwise. Then run the BIT test again to see if this corrects the problem.

Table 6-2. Fault Code Chart (continued)

Code	Explanation	Procedure
1A1A16	Not used.	
1A1A17	Not used.	
1A1A18-1 -2	NO AFSK OUTPUT NO AFSK IF.	Replace the AFSK Module Assy.
1A1A19-1	INVALID BAUD RATE	a. Check the setting of the baud rate switch on the Remote Control Interface PWB Assy and on the Audio/Microprocessor PWB Assy (in the Remote Control Unit). See paragraph 6-10c in this manual and paragraph 6-10c in the technical manual for the Remote Control Unit. b. Replace the Remote Control Interface PWB Assy.
1A1A19-2	UART LOOPBACK FAULT.	Ensure that the Remote Control Unit is turned on and then run the BIT test again. If the fault code persists, replace the Remote Control Interface PWB Assy.

Section III. REMOVAL/REPLACEMENT PROCEDURES

WARNING

Dangerous voltages exist in this ratio equipment. Before removing any covers, disconnect the primary power.

CAUTION

Use care when disconnecting ribbon cables, coaxial cables, etc.

When reassembling, insure that center conductor of coaxial cable connector does not become bent over.

NOTE

Refer to drawing FO-10 while doing the following procedures. This drawing has an apron which allows you to look at it while reading the procedures. The numbers in parentheses in the procedural steps correspond to the numbered items on the drawing. For example, "A4" refers to item 4 on view A.

NOTE

Coaxial cables are color coded the same as common resistors; the color of the cable marker corresponding to Jack number on the given circuit board.

6-9. FRONT PANEL PWB ASSY, DISPLAY ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) On the front panel, remove the AUDIO (A5), RF GAIN (A6), and SQUELCH (A7) knobs. Each knob is held in position by a pair of setscrews.

(3) Loosen the four captive Phillips screws (A1) on the front panel.

(4) Pull the front panel straight out, and swing it down into its horizontal position (views B and C).

(5) Remove the six Phillips screws (B2) holding the Remote Control Interface PWB Assy (B3), if installed. Swing the board up out of the way.

(6) Remove the nine standoffs holding the Front Panel Assy to the front panel.

NOTES

The Front Panel Assy consists of the Front Panel PWB Assy (B42) and the Display Assy (B43), which is mounted to the Front Panel PWB Assy.

Make a note of the positions of the cables before disconnecting them.

(7) Disconnect all the cables from the Front Panel Assy.

(8) Remove the Front Panel Assy from the front panel.

(9) Remove the six Phillips screws holding the Display Assy to the Front Panel PWB Assy.

b. Replacement.

(1) Using the six Phillips screws, mount the existing Display Assy to the new Front Panel PWB Assy; or mount the new Display Assy to the existing Front Panel PWB Assy.

(2) Reverse the steps of the removal procedure, beginning with step 9.

6-10. REMOTE CONTROL INTERFACE PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the four captive Phillips screws (A1) on the front panel (B41).

(3) Pull the front panel straight out, and swing it down into its horizontal position (views B and C).

(4) Remove the six Phillips screws (B2) holding the Remote Control Interface PWB Assy (B3).

NOTE

Make a note of the positions of the cables before disconnecting them.

(5) Disconnect all the cables to the Remote Control Interface PWB Assy.

(6) Remove the Remote Control Interface PWB Assy.

b. Replacement.

Reverse the order of the above steps.

c. Adjustments.

NOTE

The switch settings on the Remote Control Interface PWB Assy must match the settings for the corresponding switches on the Audio/Microprocessor PWB Assy in the Remote Control Unit.

(1) Baud Rate Select Switch, S1. This switch has 10 positions:

0 = 300 baud
1 = 600 baud
2 = 1200 baud
3 = 2400 baud
4 = 4800 baud
5 = 9600 baud
6 = not used
7 = factory test
8 = not used
9 = not used

9600 baud is the recommended setting, except when using FSK modem. In this case, set the switch for 300 baud.

(2) Interface Select Switch, S2. This switch has 10 positions:

0 = not used
1 = RS-232C (up to 100 ft.)
2 = RS-422 (up to 1 mile)
3 = FSK modem (length of phone lines)
4 = Loopback UART (factory test)

Set this switch according to the type of interface used, which is determined by the distance between the 100 Watt Transceiver and the Remote Control Unit. Maximum distance for each interface is given in parentheses.

(3) FSK Modem Hookup Select Switch, S5. This slide switch selects either two-wire or four-wire hookup for FSK modem. Set this switch for the type of hookup you have.

6-11. TRANSCEIVER CONTROL PWB ASSY.

CAUTION

The Transceiver Control PWB Assy is powered by a built-in battery which is energized even when the board is removed from the transceiver. Be careful not to lay the board on metal surfaces, tools, etc. which could cause a short circuit.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the four captive Phillips screws (A1) on the front panel (B41).

(3) Pull the front panel straight out, and swing it down into its horizontal position (views B and C).

(4) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(5) Slide the top cover toward the rear and remove it.

NOTE

Make a note of the positions of the cables before disconnecting them.

(6) Disconnect all the cables to the Transceiver Control PWB Assy (B44).

(7) Loosen the five captive Phillips screws (C9) holding the Transceiver Control PWB Assy to the chassis.

(8) Lift the Transceiver Control PWB Assy off the seven mounting pins (C10), and remove it from the transceiver.

b. Replacement.

Reverse the order of the above steps.

c. Battery Removal and Replacement.

(1) Remove the Transceiver Control PWB Assy from the chassis, as described above.

(2) Unsolder the leads of the old battery. It is not necessary to unsolder the retaining wire.

(3) Pull out the battery leads from the board and slide the battery out from under the retaining wire.

(4) Slide in the new battery, being careful to orient the positive (red) end toward the "+" silkscreened on the board.

(5) Insert the battery leads into the board and solder them, making sure that there is no slack. This ensures a strong mechanical connection.

6-12. LOW PASS FILTER PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Remove the cover (B11) over the Low Pass Filter PWB Assy.

NOTE

Make a note of the positions of the coaxial cables before disconnecting them.

(5) Disconnect the ribbon cable, the J6 connector cable, and the four coaxial cables from the Low Pass Filter PWB Assy.

(6) Loosen the nine captive Phillips screws holding the Low Pass Filter PWB Assy.

(7) Remove the Low Pass Filter PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-13. IF FILTER PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

NOTE

Make a note of the positions of the coaxial cables before disconnecting them.

(4) Disconnect the ribbon cable and the coaxial cables from the IF Filter PWB Assy (B12).

(5) Loosen the five captive Phillips screws holding the IF Filter PWB Assy.

(6) Remove the IF Filter PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-14. AFSK MODULE ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Disconnect the two coaxial cables from their destinations on the IF Filter PWB Assy (B12).

(5) Loosen the four captive Phillips screws holding the AFSK IF Filter PWB Assy (B13).

(6) Loosen the three spring-loaded, slotted captive screws (one in the front and two in the back) holding the tray (C14).

(7) Pull in on the two spring-loaded retaining pins (at the front of the tray), and swing up the tray. When the tray is above the chassis, pull it toward you and swing it all the way up until it locks in the full upright position (view C).

(8) Disconnect the two ribbon cables from the AFSK Module Assy (C15).

(9) Loosen the six captive Phillips screws (C16) holding the AFSK Module Assy.

(10) Remove the AFSK Module Assy.

b. Replacement.

Reverse the order of the above steps.

6-15. AGC/TGC PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Remove the cover (B11) over the Low Pass Filter PWB Assy.

(5) Disconnect the cable connecting to J6 on the Low Pass Filter PWB Assy.

(6) Loosen the three spring-loaded, slotted captive screws (one in the front and two in the back) holding the tray (C14).

(7) Pull in on the two spring-loaded retaining pins (at the front of the tray), and swing up the tray. When the tray is above the chassis, pull it toward you and swing it all the way up until it locks in the full upright position (view C).

(8) Disconnect the ribbon cable to the AGC/TGC PWB Assy (C17).

(9) Loosen the six captive Phillips screws (C18) holding the AGC/TGC PWB Assy.

(10) Remove the AGC/TGC PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-16. LPA/COUPLER INTERFACE PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Loosen the three spring-loaded, slotted captive screws (one in the front and two in the back) holding the tray (C14).

(5) Pull in on the two spring-loaded retaining pins (at the front of the tray), and swing up the tray. When the tray is above the chassis, pull it toward you and swing it all the way up until it locks in the full upright position (view C).

(6) Slide out the cover (C22) for the LPA/Coupler Interface PWB Assy.

(7) Loosen the three captive Phillips screws holding the LPA/Coupler Interface PWB Assy to the chassis.

(8) Unfasten the four latches (A23) holding the Transceiver Assy (A24) to the Power Supply Assy (A25).

(9) Raise up the Transceiver Assy and hold it in position with the support rod (D26).

(10) From underneath, disconnect the three ribbon cables from the LPA/Coupler Interface PWB Assy.

(11) Lift the LPA/Coupler Interface PWB Assy off its three mounting studs, and remove it from the Transceiver Assy.

b. Replacement.

Reverse the order of the above steps.

6-17. SYNTHESIZER PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Loosen the three spring-loaded, slotted captive screws (one in the front and two in the back) holding the tray (C14).

(5) Pull in on the two spring-loaded retaining pins (at the front of the upper tray), and swing up the tray. When the tray is above the chassis, pull it toward you and swing it all the way up until it locks in the full upright position (view C).

(6) Remove the cover (C19) for the Synthesizer PWB Assy.

(7) Remove the cover (C21) for the First Converter PWB Assy.

NOTE

Make a note of the positions of all cables before disconnecting them.

(8) Disconnect the coaxial cable (coming from the VCO Assy on the Synthesizer PWB Assy) from J5 on the First Converter PWB Assy.

(9) Loosen the seven captive Phillips mounting screws for the Synthesizer PWB Assy.

(10) Remove the Synthesizer PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-18. REFERENCE/BFO PWB ASSY.

NOTE

This PWB Assy has rear-mounted coaxial connectors which mate to other assemblies. Make sure that these are aligned when you are re-installing this PWB Assy.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Loosen the three spring-loaded, slotted captive screws (one in the front and two in the back) holding the tray (B14).

(5) Pull in on the two spring-loaded retaining pins (at the front of the tray), and swing up the tray. When the tray is above the chassis, pull it toward you and swing it all the way up until it locks in the full upright position (view C).

(6) Remove the cover (C20) for the Reference/BFO PWB Assy.

(7) Remove the cover (C19) for the Synthesizer PWB Assy.

NOTE

Make a note of the positions of the coaxial cables before disconnecting them.

(8) Disconnect the ribbon cables and coaxial cables from the Reference/BFO PWB Assy.

(9) From the Synthesizer PWB Assy, disconnect the cables coming from the Reference/BFO PWB Assy.

(10) Loosen the six captive Phillips mounting screws for the Reference/BFO PWB Assy.

(11) Remove the Reference/BFO PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-19. FIRST CONVERTER PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Loosen the three spring-loaded, slotted captive screws (one in the front and two in the back) holding the tray (C14).

(5) Pull in on the two spring-loaded retaining pins (at the front of the tray), and swing up the tray. When the tray is above the chassis, pull it toward you and swing it all the way up until it locks in the full upright position (view C).

(6) Remove the cover (C21) for the First Converter PWB Assy.

NOTE

Make a note of the positions of the coaxial cables before disconnecting them.

(7) Disconnect the ribbon cable and the coaxial cables from the First Converter PWB Assy.

(8) Loosen the two outboard Phillips screws holding the First Converter PWB Assy's heat sink to the chassis.

(9) Loosen the six captive Phillips mounting screws for the First Converter PWB Assy.

(10) Remove the First Converter PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-20. RECEIVER PWB ASSY.

NOTE

This PWB Assy has rear-mounted coaxial connectors which mate to other assemblies. Make sure that these are aligned when you are re-installing this PWB Assy.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Unfasten the four latches (A23) holding the Transceiver Assy (A24) to the Power Supply Assy (A25).

(3) Raise up the Transceiver Assy and hold it in position with the support rod (D26).

(4) Remove the cover (D27) for the Receiver PWB Assy.

(5) Remove the cover (D28) for the Exciter PWB Assy.

NOTE

Make a note of the positions of the coaxial cables before disconnecting them.

(6) Disconnect the ribbon cables and the coaxial cables from the Receiver PWB Assy.

(7) From the Exciter PWB Assy, disconnect the cables coming from the Receiver PWB Assy.

(8) Loosen the seven captive Phillips screws holding the Receiver PWB Assy to the Transceiver Assy.

(9) Remove the Receiver PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-21. EXCITER PWB ASSY.

NOTE

This PWB Assy has rear-mounted coaxial connectors which mate to other assemblies. Make sure that these are aligned when you are re-installing this PWB Assy.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Unfasten the four latches (A23) holding the Transceiver Assy (A24) to the Power Supply Assy (A25).

(3) Raise up the Transceiver Assy and hold it in position with the support rod (D26).

(4) Remove the cover (D28) for the Exciter PWB Assy.

(5) Remove the cover (D27) for the Receiver PWB Assy.

NOTE

Make a note of the positions of the coaxial cables before disconnecting them.

(6) Disconnect the ribbon cables and the coaxial cables from the Exciter PWB Assy.

(7) From the Receiver PWB Assy, disconnect the cables coming from the Exciter PWB Assy.

(8) Loosen the eight captive Phillips screws holding the Exciter PWB Assy to the Transceiver Assy.

(9) Remove the Exciter PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-22. 13.6 V POWER SUPPLY ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Unfasten the four latches (A23) holding the Transceiver Assy (A24) to the Power Supply Assy (A25).

(3) Raise up the Transceiver Assy and hold it in position with the support rod (D26).

(4) Loosen the two 1/4-turn fasteners at the front of the lower cover (D29). Remove the lower cover by lifting it up and sliding it forward.

(5) Loosen the four 1/4-turn fasteners (D30) on the 13.6 V Power Supply Assy cover (D31), and remove the cover.

(6) Loosen the four spring-loaded, slotted captive screws inside the 13.6 V Power Supply Assy.

(7) Disconnect the three plugs on the wires exiting the rear of the EMI Filter Assy (D32), disconnect the J3 connector on the Power Supply Protection and Control PWB Assy (D33) and disconnect the ground connection.

(8) Remove the 13.6 V Power Supply Assy from the Power Supply Assy (A25).

(9) On the inside of the 13.6 V Power Supply Assy, remove the mounting nuts for the EMI Filter Assy.

(10) Disconnect the wires emerging from the side of the EMI Filter Assy from their destinations inside the 13.6 V Power Supply Assy.

(11) Remove the EMI Filter Assy from the 13.6 V Power Supply Assy.

a. Replacement.

(1) Use the mounting nuts to fasten the existing EMI Filter Assy to the new 13.6 V Power Supply Assy, and reconnect the EMI Filter Assy wires to their proper destinations inside the 13.6 V Power Supply Assy.

(2) Reverse the steps of the removal procedure, beginning with step 8.

6-23. POWER SUPPLY PROTECTION AND CONTROL PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Unfasten the four latches (A23) holding the Transceiver Assy (A24) to the Power Supply Assy (A25).

(3) Raise up the Transceiver Assy and hold it in position with the support rod (D26).

(4) Loosen the two 1/4-turn fasteners at the front of the lower cover (D29). Remove the lower cover by lifting it up and sliding it forward.

NOTE

Make a note of the positions of the plugs and wires before disconnecting them.

(5) Disconnect all the plugs from the Power Supply Protection and Control PWB Assy (D33). Disconnect the wires and the three pronged terminal plate from the terminal strip on the board.

(6) Loosen the six captive Phillips screws on the Power Supply Protection and Control PWB Assy.

(7) Remove the Power Supply Protection and Control PWB Assy.

b. Replacement.

Reverse the order of the above steps.

6-24. POWER AMPLIFIER ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Disconnect the ribbon cable for the Power Amplifier Assy at J8 on the Interconnect PWB Assy (B35).

(5) Loosen the two captive Phillips screws holding the Power Amplifier Assy (B34) to the rear of the chassis.

(6) Gently move the Power Amplifier Assy away from the chassis, disconnect the two coaxial cables from the circuit board, and disconnect the power cable.

(7) Remove the Power Amplifier Assy.

b. Replacement.

Reverse the order of the above steps.

6-25. MULTIVOLTAGE SUPPLY ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Loosen the two captive slotted screws holding the Multivoltage Supply Assy (B36) to the mounting bracket.

(5) Disconnect the power plug, and lift out the Multivoltage Supply Assy.

(6) Remove the Multivoltage Supply Assy.

b. Replacement.

Reverse the order of the above steps.

6-26. CRYSTAL OSCILLATOR ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Loosen the three 1/4-turn fasteners (A8) on the top cover (A37).

(3) Slide the top cover toward the rear and remove it.

(4) Unfasten the four latches (A23) holding the Transceiver Assy (A24) to the Power Supply Assy (A25).

(5) Raise up the Transceiver Assy and hold it in position with the support rod (D26).

(6) Disconnect the coaxial cable and the wired cable from the Crystal Oscillator Assy (D38).

(7) Remove the four nuts (D40) holding the Crystal Oscillator Assy to its mounting bracket.

(8) Reach over and remove the Crystal Oscillator Assy (B39) through the top of the transceiver.

b. Replacement.

Reverse the order of the above steps.

6-27. AUDIO INTERFACE PWB ASSY.

a. Removal.

(1) Disconnect the input power from the 100 Watt Transceiver.

(2) Disconnect the wires from TB1 at the rear of the 100 Watt Transceiver.

(3) Loosen the two large captive Phillips screws holding the Audio Interface PWB Assy (B45) to the rear of the 100 Watt Transceiver.

(4) Pull out the Audio Interface PWB Assy, and disconnect the two ribbon cables.

(5) Remove the Audio Interface PWB Assy from the 100 Watt Transceiver.

b. Replacement.

Reverse the order of the above steps.

c. Switch Settings.

NOTE

The switch settings on the Audio Interface PWB Assy in the 100 Watt Transceiver must match the switch settings on the Audio Interface PWB Assy in the Remote Control Unit.

(1) 2-Wire/4-Wire PATCH Select Switch, S1

Set this switch to the 2-wire (2W) or 4-wire (4W) position, according to the number of wires connected to the PATCH terminals at the terminal strip (TB1) on the Audio Interface PWB Assy.

(2) 2-Wire/4-Wire LINE Select Switch, S2

Set this switch to the 2-wire (2W) or 4-wire (4W) position, according to the number of wires connected to the LINE terminals at the terminal strip (TB1) on the Audio Interface PWB Assy.

Section IV. PERIODIC MAINTENANCE PROCEDURES

6-28. PERIODIC MAINTENANCE ACTIONS. The 100 Watt Transceiver requires only a limited amount of periodic maintenance. The following actions are recommended at the intervals listed. During any of the specific procedures listed, take note of any unusual equipment conditions which may indicate degrading or degraded performance, and make the necessary corrections.

a. Clean Air Filter. Clean the equipment air filter every 56 days of equipment operation, or sooner if filter is noticeably soiled.

b. Visual Inspection. Every 56 days of equipment operation, inspect the transceiver for signs of overheating, particularly, the Low Pass Filter Assembly, A1A5. Observe that dust build-up is not excessive within the unit, particularly in the Power Supply Unit, A2.

c. Frequency Check. Every 336 days, verify the frequency accuracy of the transceiver and adjust the Crystal Oscillator Assy, A1A8, as required. For this adjustment, a frequency counter locked to a very accurate house-standard should be used, since a typical frequency counter may be less accurate than the standard within the 100 Watt Transceiver. See Section V, Alignment Procedures, for instructions on how to check and adjust the Crystal Oscillator Assy.

WARNING

Do not dispose of lithium batteries in the trash. These batteries contain hazardous materials that can contaminate the environment.

d. Memory Battery Replacement. The memory battery used to power the channel and operating parameters memory device should be replaced as required. This battery is located on the Transceiver Control PWB Assy, A1A12. For instructions on removing and replacing this battery, see the removal and replacement procedure for the Transceiver Control PWB Assy. Note that the projected life of the battery is ten years.

Section V. ALIGNMENT PROCEDURES

6-29. INTRODUCTION. This section contains instructions for checking and adjusting the replaceable subassemblies in the 100 Watt Transceiver. This section also contains circuit board layouts to help you identify the components that can be adjusted. To do the procedures described in this section, you need the test equipment listed in Table 6-3 or equivalents. Refer to figure 1-3 for subassembly locations.

Table 6-3. Test Equipment*

Generic Name	Military Designation	Manufacturer, Model No.	Federal Stock No.	Required Range
Oscilloscope		Tektronix, Model 465m		5 mV to 200 V AC or DC; DC to 100 MHz
Signal Generator (RF)		Hewlett Packard, Model 8640B		-120 to +20 dBm; 440 KHz to 70.5 MHz in 10 Hz increments
Signal Generator (audio)		Hewlett Packard, Model 204D		-70 to +10 dBm; 300 Hz to 3.3 KHz
Electronic Voltmeter w/ AC Probe & T-connector		Hewlett Packard, Model 410C Model 11036A Model 11042A		10 to 100 V rms; 1.6 to 30 MHz (peak reading)
AC Voltmeter		Hewlett Packard, Model 400F		300 uV to 3 V (audio frequency)
Digital Multimeter		Fluke, Model 8012A		200 mV to 250 Vac; 200 mV to 40 Vdc; 0 to 20 megohms
Spectrum Analyzers		Hewlett Packard, Model 140T (display) Model 8553B (RF) Model 8552B (IF)		-70 to +20 dBm; 455 KHz to 70.5 MHz
10:1 Probe (for oscilloscope)		Hewlett Packard, Model 1008DA		Input impedance: 1 megohm
10 dB Pad		AB10N		

* NOTE: Equivalent Items Authorized

Table 6-3. Test Equipment (continued)

Generic Name	Military Designation	Manufacturer, Model No.	Federal Stock No.	Required Range
In-Line fuse		Hewlett Packard, Model 11509A		DC-480 MHz
Frequency Counter*		Hewlett Packard, Model 5335A		Calibrate 10 MHz to within 1 part in 10^9
DC Power Supply		Hewlett Packard, Model 6200B		0 - 12 Vdc at 1.5 amps
Dummy Load		Bird, Model 8833		100 W, 50 ohms,
Wattmeter		Thruline Model 43		

* Must be connected to an external frequency standard with a stability of at least 1 part in 10^9 per day.

6-30. ALIGNMENT PROCEDURES.

NOTE

After each of the following alignments, disconnect test equipment and reconfigure equipment (module or circuit card) to normal operating condition.

NOTE

Disconnect LPA, antenna coupler, and remote control unit before performing alignments. Connect transceiver to dummy load.

a. EXCITER PWB ASSY., A1A1 (figure 6-3).

(1) R110/R117, Carrier Null Adjustments

(a) Disconnect A1A7J3 from P1. Connect a spectrum analyzer to P1, with setup as follows:

- Input Attn.....20 DB
- Scan Width.....0.5 KHZ/Div.*
- Band Width.....0.1 KHZ
- Scan Time/Div.....0.1 Sec
- Log Ref Level.....-30 dBm
- Scan Trigger.....Auto
- Scan Mode.....Int
- Video Fltr.....Off
- Log/Linear.....10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(b) Key the transceiver in CW mode with the CW key.

(c) You should see a signal something like Figure 6-2.

(d) Adjust R110 and R117 for a minimum carrier level (at least 40 dB down from sidetones).

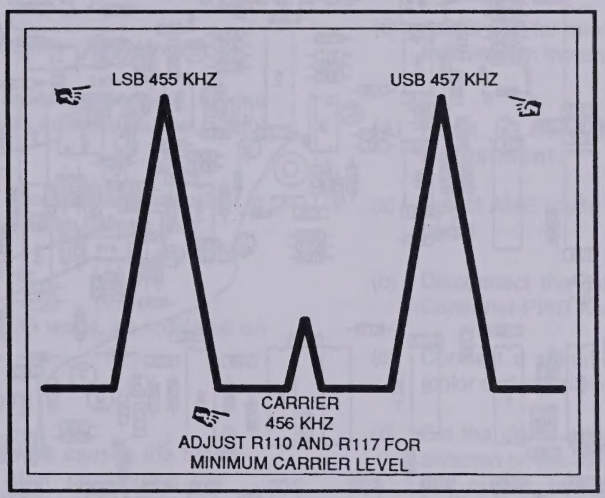
(2) L7, 455 KHZ Presence Det Peaking Adj.

(a) Using a signal generator, inject an unmodulated 455 KHz, -28 dBm signal into P2.

(b) Connect J3 to a 50 ohm dummy load.

NOTE

THE ILLUSTRATION BELOW ASSUMES THAT SWITCH S1 ON IF FILTER PWB A1A2 IS IN THE UPPER SIDE BAND POSITION (U). IF S1 IS IN THE LOWER SIDE BAND POSITION (L), THE FREQUENCIES SHOWN WILL BE SHIFTED DOWNWARD BY 2 KHZ.



*350-074

Figure 6-2. Carrier Null Adjustment.

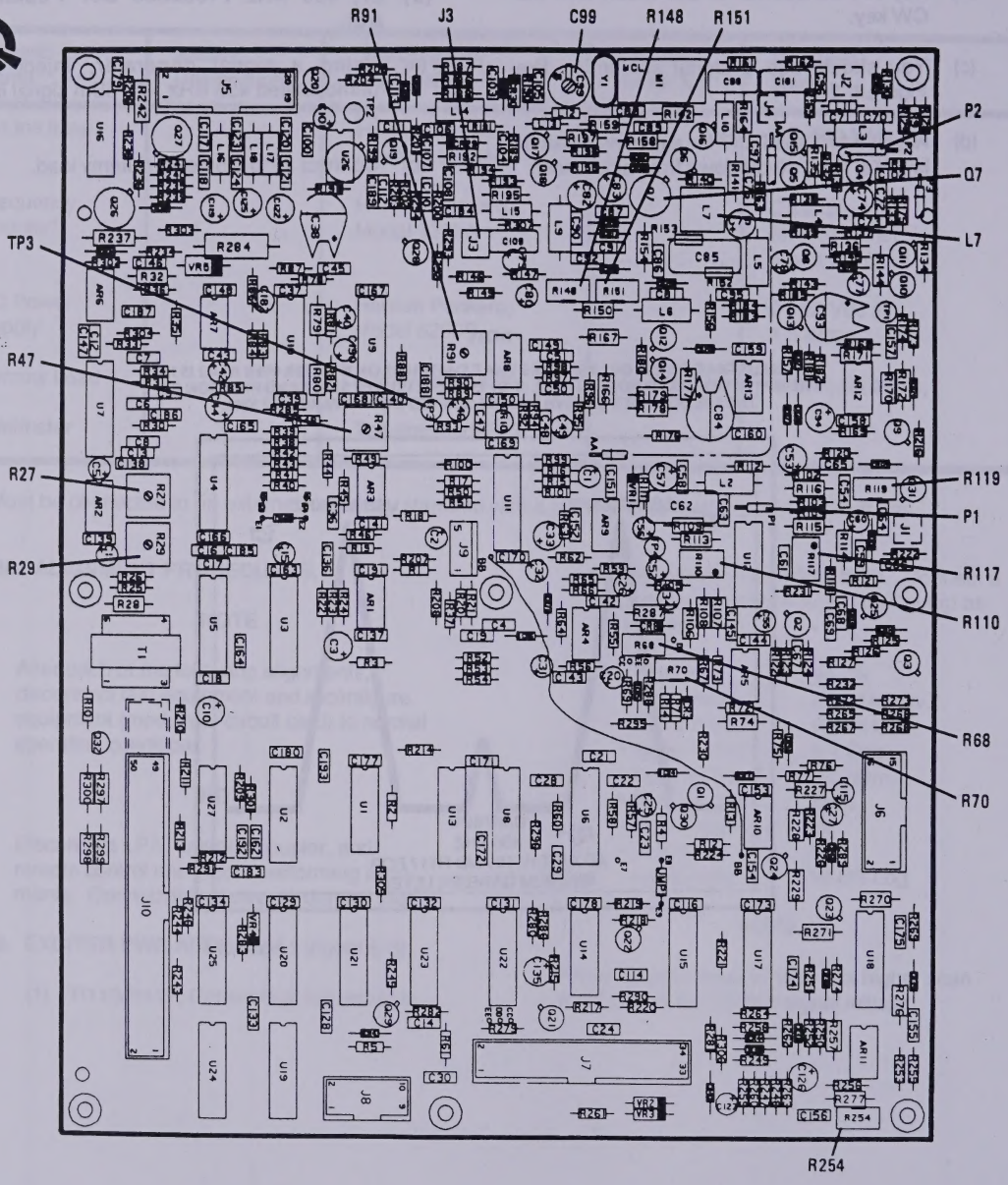


Figure 6-3. Exciter PWB Assy.

(c) Observe the collector of Q7 with an oscilloscope.

(d) Adjust L7 for the peak signal on the oscilloscope.

(3) R119, AME Inserted Carrier Level Adjustment

(a) Connect J1 (RF in/out) of the transceiver to a wattmeter and 50 ohm dummy load.

(b) Key the transceiver in AME mode with no modulation.

(c) Adjust R119 for a level of 25 watts on the wattmeter.

(4) R148, Tune Power Adjustment

(a) Connect an antenna coupler to the transceiver with an antenna coupler control cable.

(b) Connect J1 (RF in/out) of the transceiver to a wattmeter and 50 ohm dummy load.

(c) Key the transceiver.

(d) Adjust R148 for 35 watts, as indicated on the meter.

NOTE

Performing this adjustment causes the tune power to lock up. After completing the adjustment, turn the transceiver off and on again to reset the tune power flag.

(5) C99, Bandstop Filter Adjustment

(a) Connect a spectrum analyzer to J3, with a 10 dB attenuator pad between the analyzer and J3. Setup as follows:

- Input Attn.....50 DB
- Scan Width.....0.5 KHZ/Div.*
- Band Width.....0.3 KHZ
- Scan Time/Div.....50 msec
- Log Ref Level.....+10 dBm
- Scan Trigger.....Auto
- Scan Mode.....Int
- Video Fltr.....Off
- Log/Linear.....10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(b) Using a signal generator, inject an unmodulated 454 KHz signal at -18 dBm into P2.

(c) Key the transceiver, and observe the signal on the spectrum analyzer. 40.454 MHz signal will be observed.

(d) Adjust C99 for maximum signal strength, as indicated on the analyzer.

(6) R254, Low Power Threshold Adjustment.

(a) Select AME mode on the transceiver front panel.

(b) Disconnect the cable from J4 on the First Converter PWB Assy.

(c) Connect a signal generator to this cable (color coded yellow).

(d) Set the signal generator for the frequency selected on the transceiver front panel. Set the output level to -20 dBm, with a modulating tone of 1 KHz at 30% modulation.

(e) Key the transceiver with the 2ND, TX KEY buttons on the front panel. Set meter to FWD.

(f) Adjust the signal generator level so that the output power of the transceiver is 50 W, as indicated on the front panel meter.

(g) Adjust R254 so that the LOW PWR Indicator just comes on.

(7) R47 , Audio Meter Calibration Adjustment.

(a) Select the AUDIO meter on the transceiver front panel.

(b) Select CW mode.

(c) Key the transceiver with the CW key, and adjust R47 for 0 dB on the meter.

(8) R27 (LINE) and R29 (AUDIO 2), Leveling Adjustments.

These potentiometers are used to compensate for varying input levels in these signals. Adjust them as follows:

(a) For AUDIO 2, inject a 1 KHz signal at +10 dBm into J4, pins 4 and 5, at the rear of the transceiver. For LINE, connect the Remote Control Unit's control cable into J9 at the rear of the transceiver.

(b) For AUDIO 2, select AUDIO 2 as the audio source on the transceiver front panel. For LINE, select REMOTE operation and audio source of MIC on the transceiver front panel.

(c) Select the AUDIO meter on the transceiver front panel (for AUDIO 2) or on the Remote Control Unit (for LINE).

(d) Key the transceiver, and adjust R29 (AUDIO 2) or R27 (LINE) for an indication of 0 on the transceiver meter. (For the LINE adjustment, you will have to talk into the microphone on the Remote Control Unit.)

(9) R68 (CW) and R70 (VOX), Delay Adjustments.

These potentiometers set the "hang time" for VOX and CW keying; that is, they determine the amount of time it takes for the transceiver to unkey. These adjustments are preferential, but the normal factory setting is 1/2 to 3/4 second for VOX voice and 1 second for CW.

(a) To adjust R68 select CW mode and connect a CW key, estimate the elapsed time before the transceiver unkeys. Adjust R68 until the desired time delay is achieved.

(b) Using MIC as the AUDIO SOURCE, adjust R70 so that the end of a test.count, the desired time elapses before the transceiver unkeys.

(10) R91, Clipper Level Adjustment.

This adjustment is preferential. The range is from 0 dB (no clipping, R91 fully counterclockwise) to 12 dB (maximum clipping, R91 fully clockwise), with the normal factory setting at 6 dB. To obtain this factory setting, do the following:

NOTE

A close approximation to the following adjustment can be obtained by simply setting R91 to the center of its turning range.

(a) Select CLIP on the transceiver.

(b) Connect an oscilloscope to TP3 on the Exciter PWB Assy.

(c) Connect an audio signal generator to PATCH IN on the rear panel terminal strip of the transceiver.

(d) Select PATCH as the AUDIO SOURCE on the transceiver. (Make sure that the Audio Interface PWB Assy is set for 4-wire PATCH.)

(e) Turn R91 fully counterclockwise.

(f) Set the signal generator frequency to 1 KHz. Adjust the signal generator level for a 1 V pk-pk signal on the oscilloscope. Oscilloscope is still connected to TP3.

(g) Turn R91 clockwise until the signal on the oscilloscope increases to 2 V pk-pk.

b. IF FILTER PWB ASSY., A1A2 (figure 6-4)

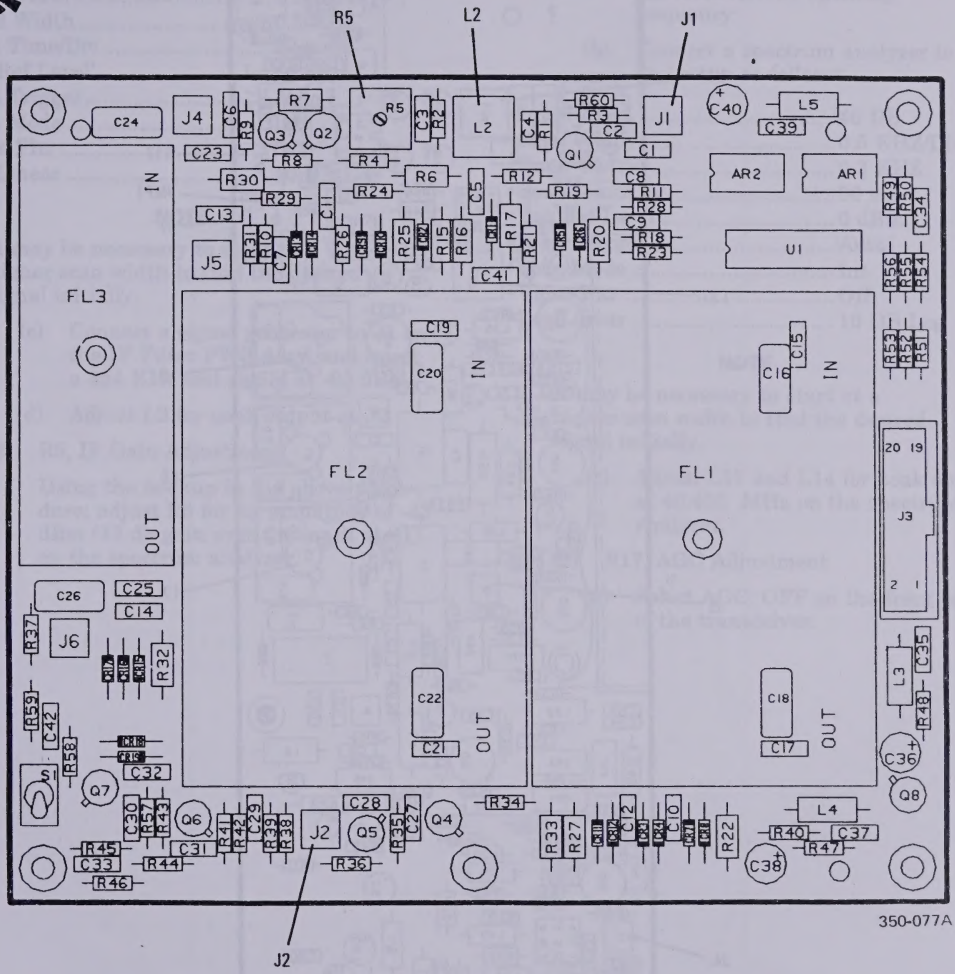


Figure 6-4. IF Filter PWB Assy.

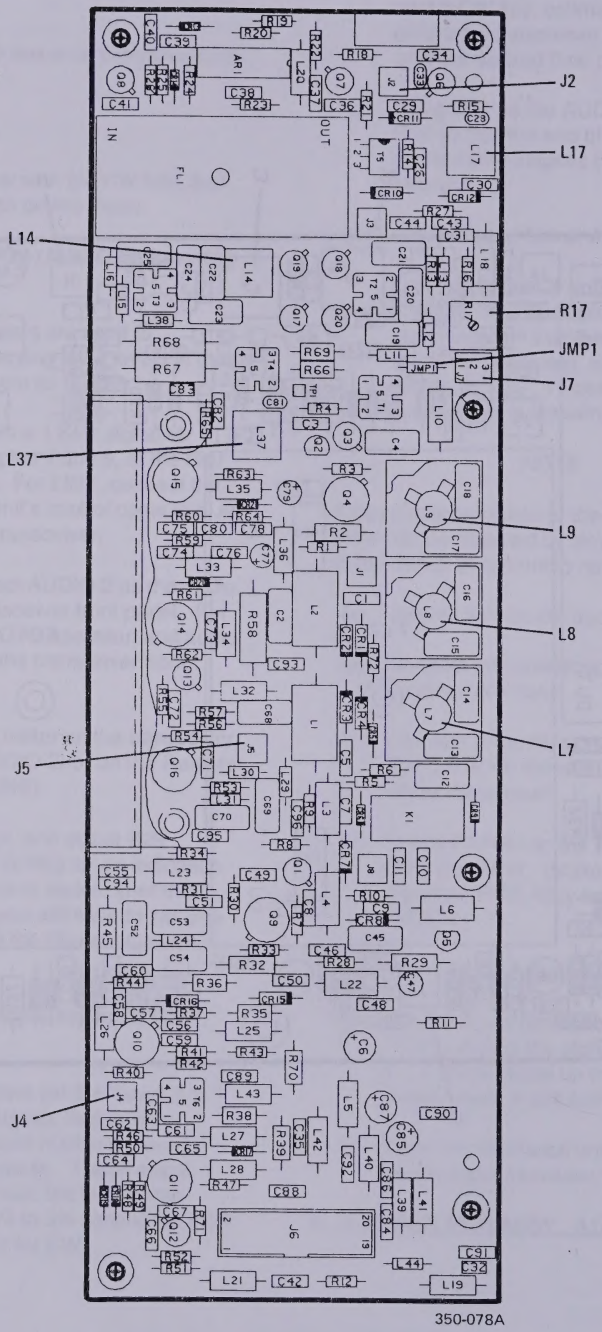


Figure 6-5. First Converter PWB Assy.

(1) L2, 455 KHZ Fltr Input Adj.

(a) Select USB mode on the transceiver.

(b) Connect a spectrum analyzer to J2 on the IF Filter PWB Assy. and setup as follows:

- Input Attn ..... 0 DB
- Scan Width ..... 1 KHZ/Div*
- Band Width ..... 0.3 KHZ
- Scan Time/Div ..... 50 msec
- Log Ref Level ..... 40 dBm
- Scan Trigger ..... Auto
- Scan Mode ..... Int
- Video Fltr ..... Off
- Log/Linear ..... 10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(c) Connect a signal generator to J1 on the IF Filter PWB Assy, and inject a 454 KHz test signal at -60 dBm.

(d) Adjust L2 for peak output at J2.

(2) R5, IF Gain Adjustment

Using the hookup in the above procedure, adjust R5 for an amplitude of -43 dBm (17 db gain over the input at J1) on the spectrum analyzer.

c. FIRST CONVERTER PWB ASSY A1A3 (figure 6-5).

(1) Deleted

(2) L17, and L14, 40 MHZ IF Fltr Peaking Adj.

(a) Inject a -20 dBm signal into J1 at the transceiver's operaing frequency.

(b) Connect a spectrum analyzer to J2 and setup as follows:

- Input Attn ..... 40 DB
- Scan Width ..... 0.5 KHZ/Div*
- Band Width ..... 0.3 KHZ
- Scan Time/Div ..... 50 msec
- Log Ref Level ..... 0 dBm
- Scan Trigger ..... Auto
- Scan Mode ..... Int
- Video Fltr ..... Off
- Log/Linear ..... 10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(c) Adjust L17 and L14 for peak output at 40.455 MHz on the spectrum analyzer.

(3) R17, AGC Adjustment

(a) Select AGC: OFF on the front panel of the transceiver.

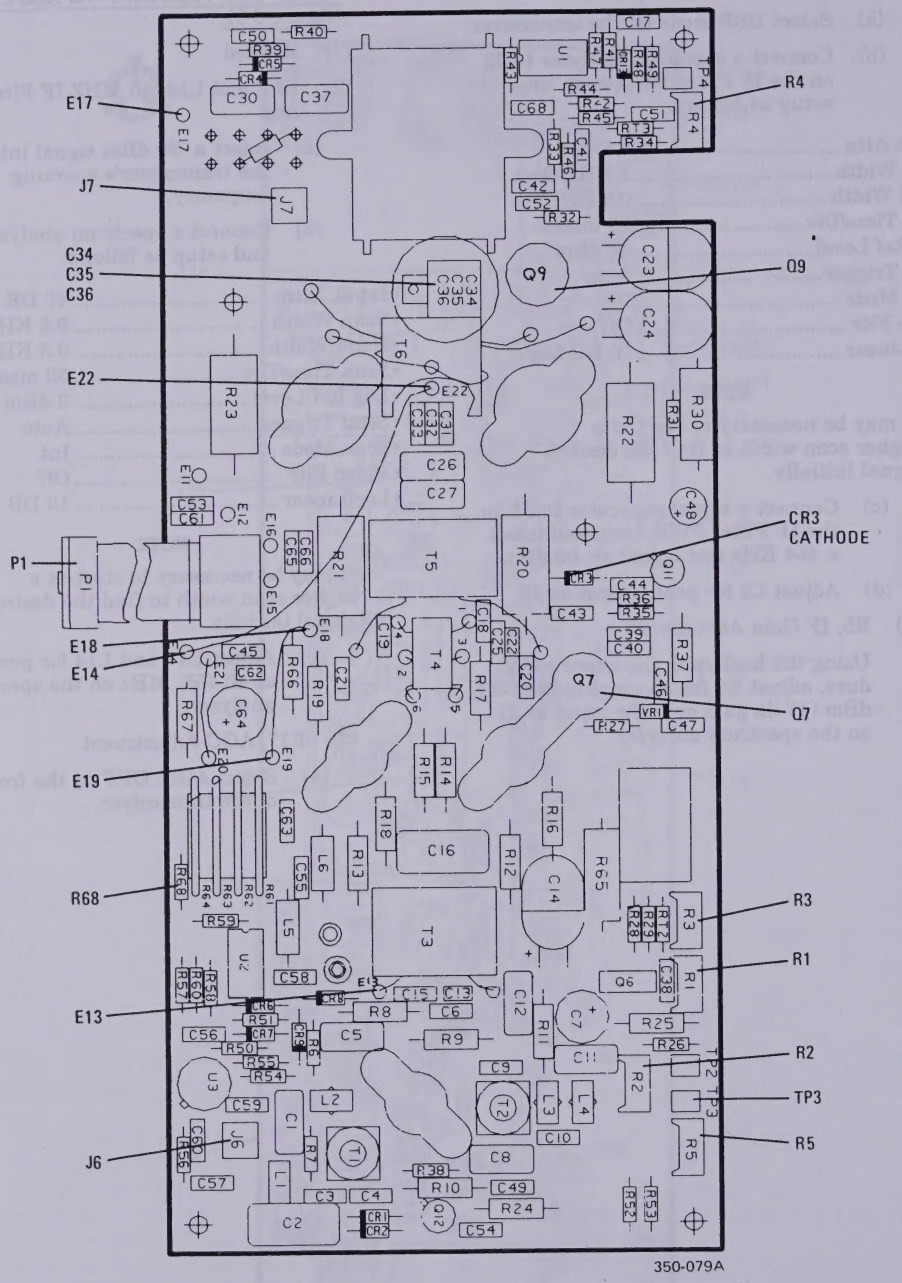


Figure 6-6. Power Amplifier PWB.

(b) Set the RF GAIN control on the front panel fully clockwise.

(c) Connect a spectrum analyzer to J2. Setup as follows:

- Input Attn.....40 DB
- Scan Width.....0.5 KHZ/Div.*
- Band Width.....0.3 KHZ
- Scan Time/Div.....50 msec
- Log Ref Level.....0 dBm
- Scan Trigger.....Auto
- Scan Mode.....Int
- Video Fltr.....Off
- Log/Linear.....10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially

(d) Inject a -30 dBm signal at the operating frequency into J1 (RF in/out) on the back of the transceiver.

(e) Observe the level of the 40.455 MHz signal on the analyzer.

(f) Rotate the RF GAIN control fully counter-clockwise.

(g) Adjust R17 so that the signal on the analyzer is 20 dB less than it was when the RF GAIN control was fully clockwise.

(4) L37, 40 MHZ If Trap Adj.

(a) Inject a 0 dBm signal at 40.455 MHz into J5.

(b) Connect a spectrum analyzer to J2. Setup as follows:

- Input Attn.....40 DB
- Scan Width.....0.5 KHZ/Div.*
- Band Width.....0.3 KHZ
- Scan Time/Div.....50 msec
- Log Ref Level.....0 dBm
- Scan Trigger.....Auto
- Scan Mode.....Int
- Video Fltr.....Off
- Log/Linear.....10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(c) With no signal coming in at J1, adjust L37 for minimum signal indication on the spectrum analyzer at 40.455 MHz.

d. POWER AMPLIFIER A1A4 (figure 6-6).

Deleted

Do not perform at organization level maintenance.

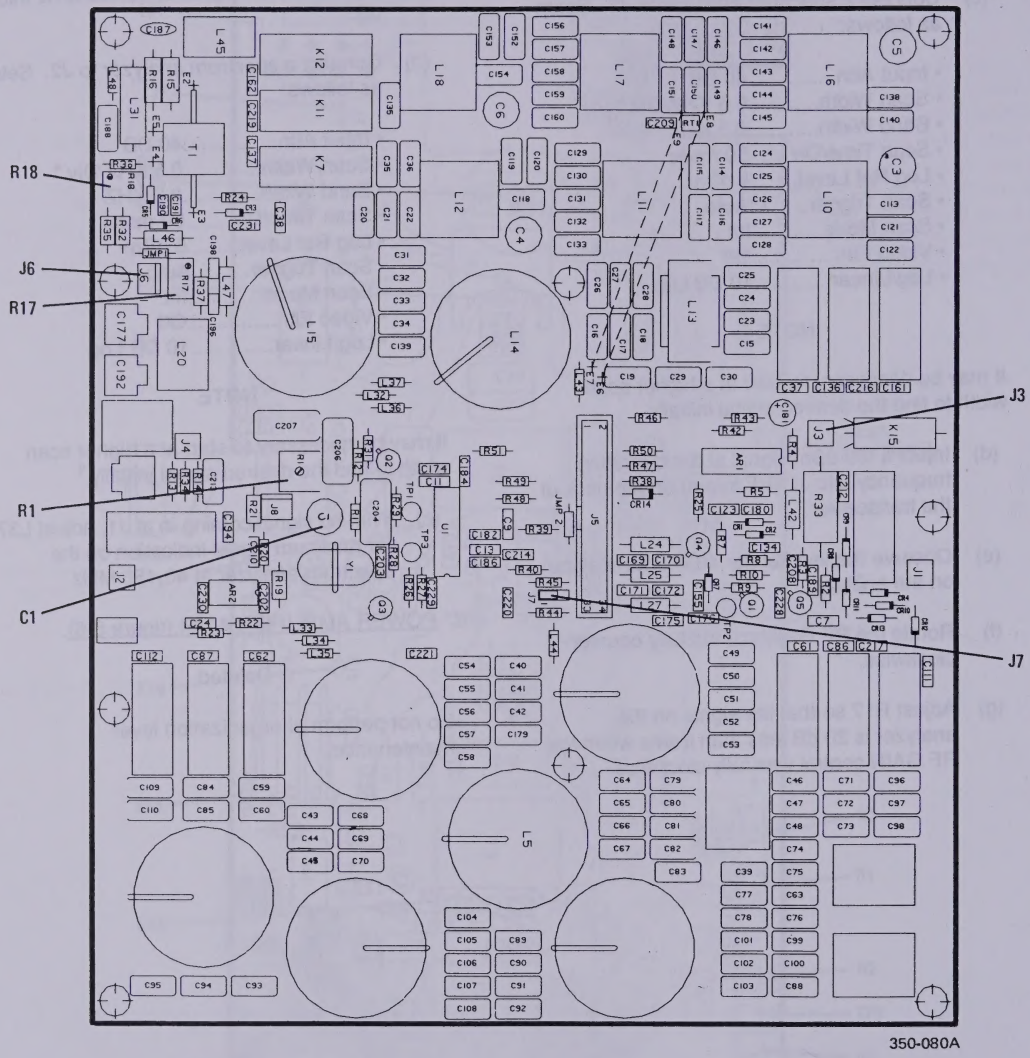


Figure 6-7. Low Pass Filter PWB Assy.

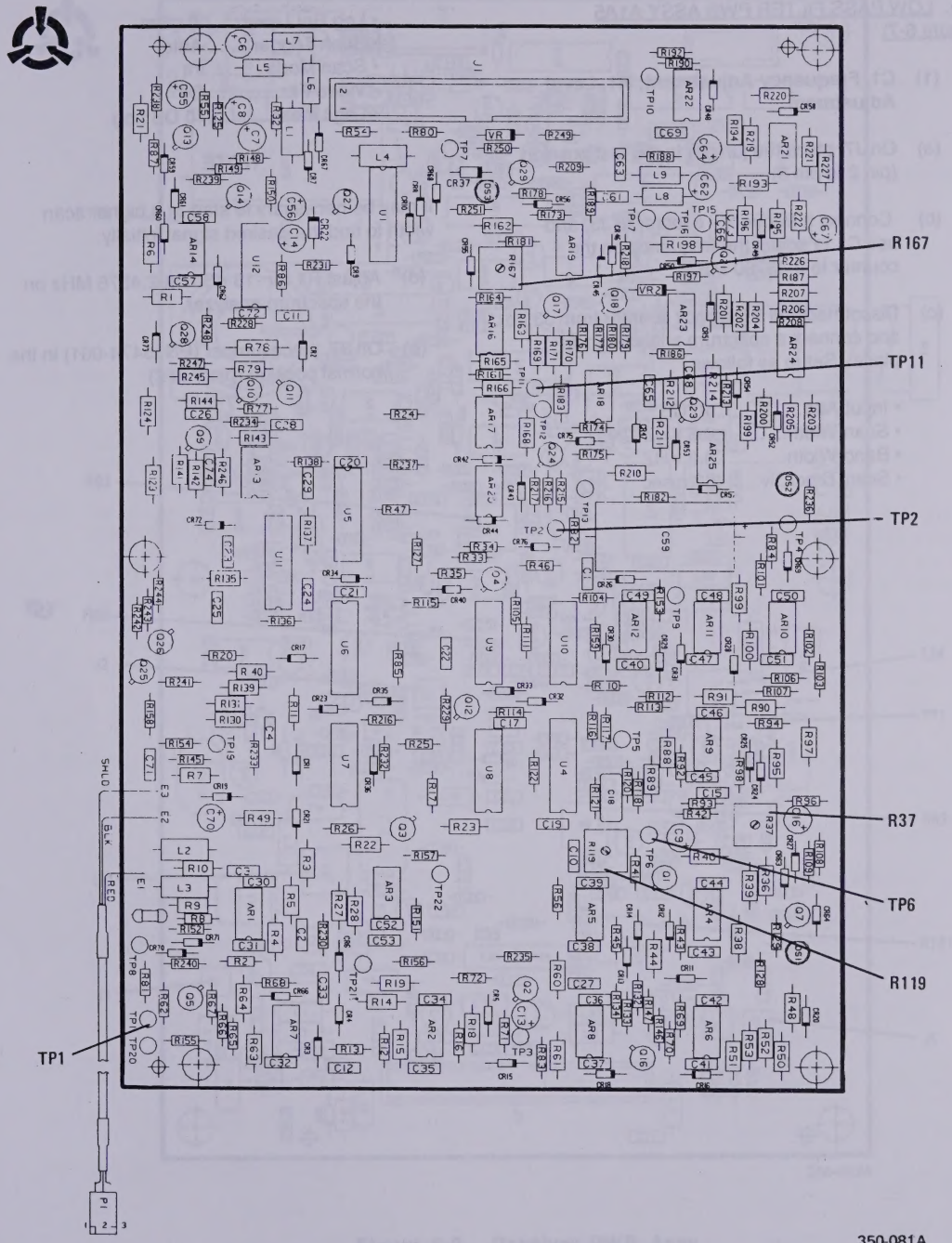


Figure 6-8. AGC/TGC PWB Assy.

e. LOW PASS FILTER PWB ASSY A1A5 (figure 6-7)

(1) C1, Frequency Adjustment; R1, Level Adjustment.

(a) On J7, place the jumper in the test position (pin 2 to pin 3).

(b) Connect a frequency counter to J3, and use C1 to adjust the frequency on the counter to 2.45760 MHz.

(c) Disconnect the frequency counter from J3, and connect a spectrum analyzer in its place. Setup as follows:

- Input Attn.....40 DB
- Scan Width.....0.5 KHZ/Div.*
- Band Width.....0.3 KHZ
- Scan Time/Div.....50 msec
- Log Ref Level.....0 dBm
- Scan Trigger.....Auto
- Scan Mode.....Int
- Video Fltr.....Off
- Log/Linear.....10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(d) Adjust R1 for -18 dBm at 2.4576 MHz on the spectrum analyzer.

(e) On J7, place jumper (PN65474-001) in the normal position (pin 1 to 2).

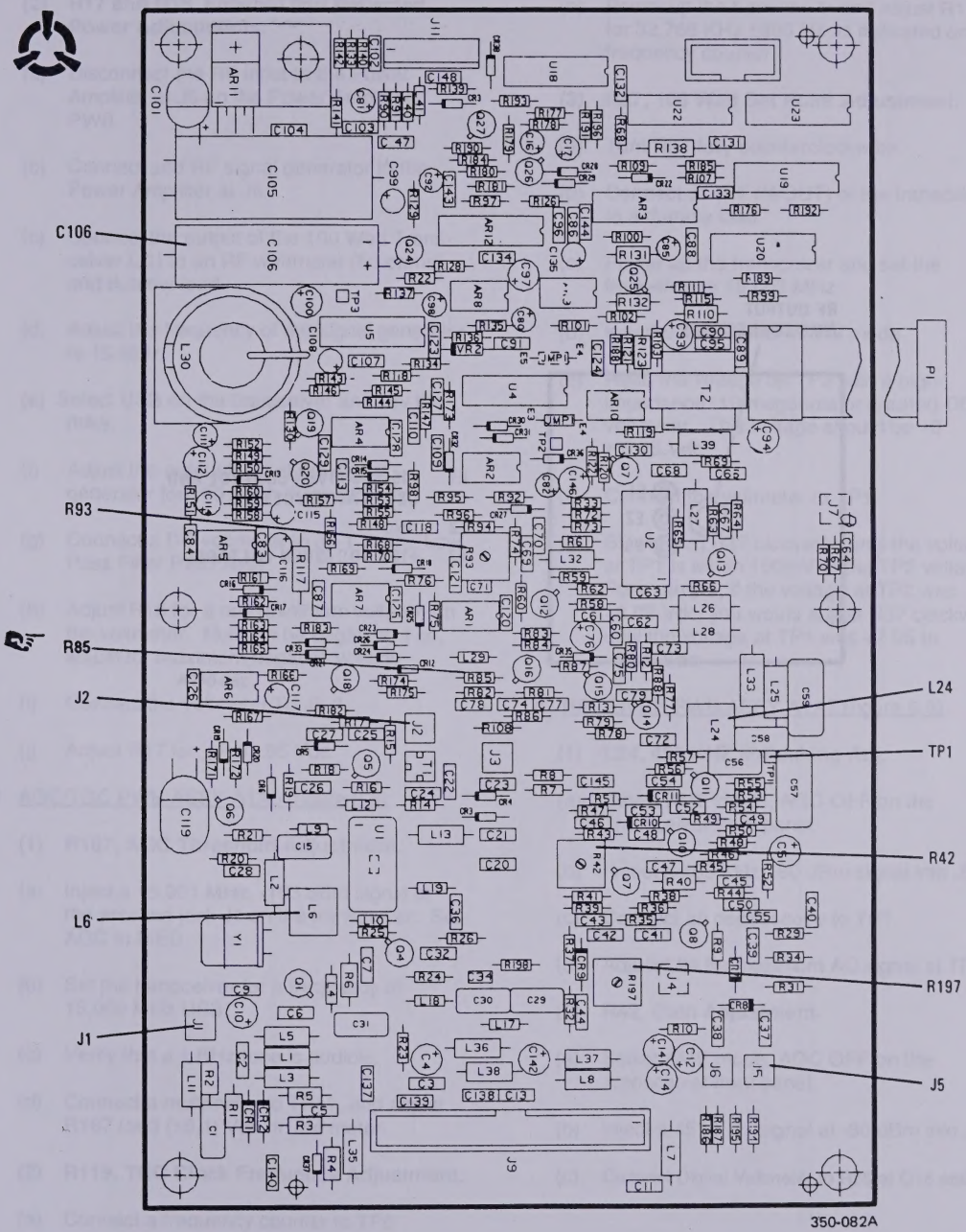
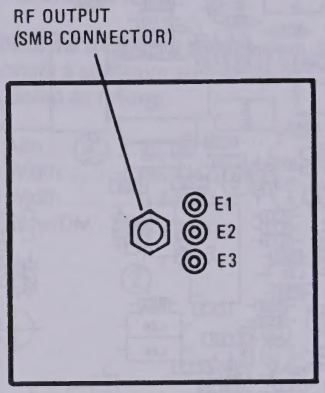


Figure 6-9. Receiver PWB Assy.



E1 +15 VDC (OVEN CONTROL AND OSCILLATOR VOLTAGE)
E2 GND
E3 +13.6 VDC (OVEN VOLTAGE)

350-049A

Figure 6-10. Crystal Oscillator Assembly (Bottom View).

(2) R17 and R18, Forward and Reflected Power Adjustments.

(a) Disconnect the RF input to the Power Amplifier at J6 on the Power Amplifier PWB.

(b) Connect and RF signal generator to the Power Amplifier at J6.

(c) Connect the output of the 100 Watt Transceiver (J1) to an RF wattmeter (50 ohms) and dummy load.

(d) Adjust the frequency of the signal generator to 15 MHz.

(e) Select USB on the transceiver and key the mike.

(f) Adjust the output level of the signal generator for 100 W on the wattmeter.

(g) Connect a DC voltmeter to J6-1 on the Low Pass Filter PWB Assy.

(h) Adjust R18 for a null (minimum voltage) on the voltmeter. Null can be negative; if so, adjust for maximum negative voltage.

(i) Connect the voltmeter To J6-2.

(j) Adjust R17 for + 8.0 ±05 Vdc.

f. AGC/TGC PWB ASSY A1A6 (figure 6-8).

(1) R167, AGC Threshold Adjustment.

(a) Inject a 15.001 MHz, -103 dBm signal at the antenna jack J1 on the transceiver. Set AGC to MED.

(b) Set the transceiver for a frequency of 15.000 MHz USB.

(c) Verify that a 1 KHz tone is audible.

(d) Connect a multimeter to TP11, and adjust R167 for 0 (±0.1) Vdc on the meter.

(2) R119, TGC Clock Frequency Adjustment.

(a) Connect a frequency counter to TP6.

(b) Power up the transceiver and adjust R119 for 32.768 KHz ±800 Hz as indicated on the frequency counter.

(3) R37, 100 Watt Set Point Adjustment.

(a) Turn R37 fully counterclockwise.

(b) Connect J1 (RF IN/OUT) of the transceiver to a dummy load.

(c) Power up the transceiver and set the frequency to 15,000 MHz.

(d) Key the transceiver in CW mode.

(e) Read the voltage on TP2 with a high-impedance (10 megohms or greater) DC voltmeter. This voltage should be +8 ± 0.25 Vdc.

(f) Connect the voltmeter to TP1.

(g) Slowly turn R37 clockwise until the voltage at TP1 is within 100mV of the TP2 voltage. For example, if the voltage at TP2 was +8.05 Vdc, you would adjust R37 clockwise until the voltage at TP1 was +7.95 to +8.15 Vdc.

g. RECEIVER PWB ASSY A1A7 (figure 6-9).

(1) L24, 455 KHZ IF Peaking Adj.

(a) Select AME mode, AGC OFF on the transceiver front panel.

(b) Inject a 455 KHz, -80 dBm signal into J5.

(c) Connect an oscilloscope to TP1.

(d) Adjust L24 for maximum AC signal at TP1.

(2) R42, Gain Adjustment.

(a) Select AME mode, AGC OFF on the transceiver front panel.

(b) Inject a 455 KHz signal at -80 dBm into J5.

(c) Connect Digital Voltmeter to R85 at Q16 end.

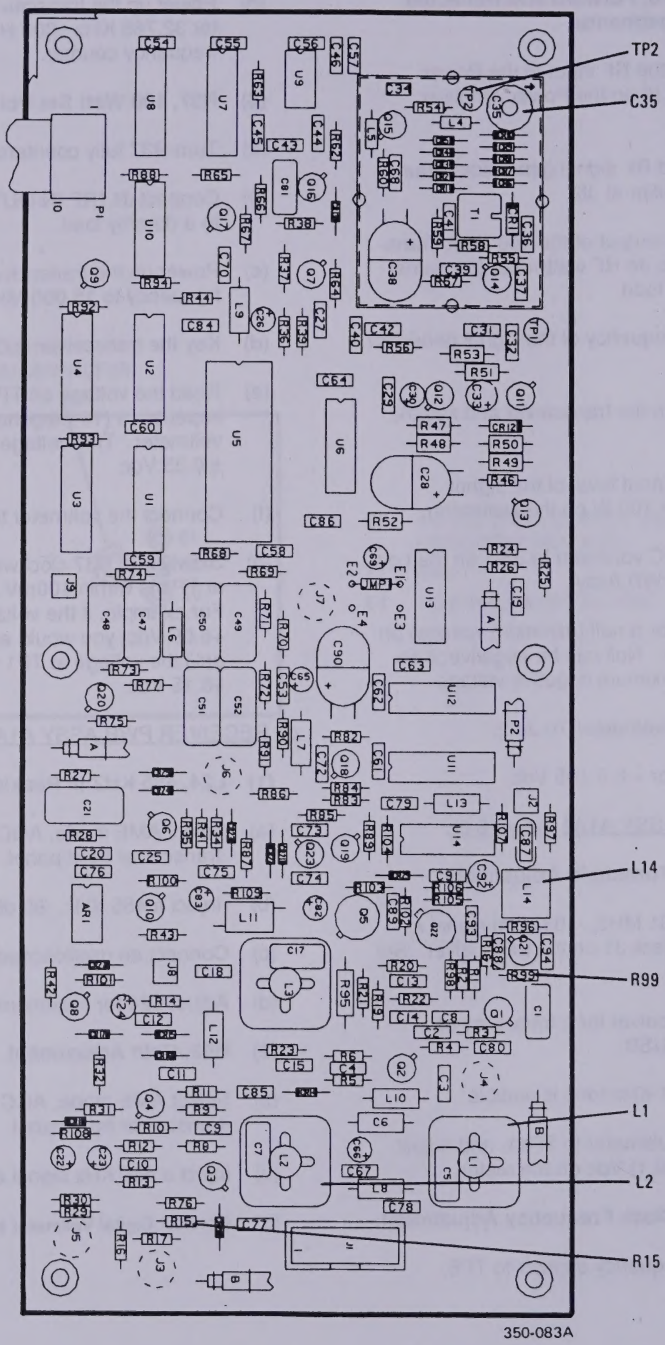


Figure 6-11. Reference/BFO PWB Assy.

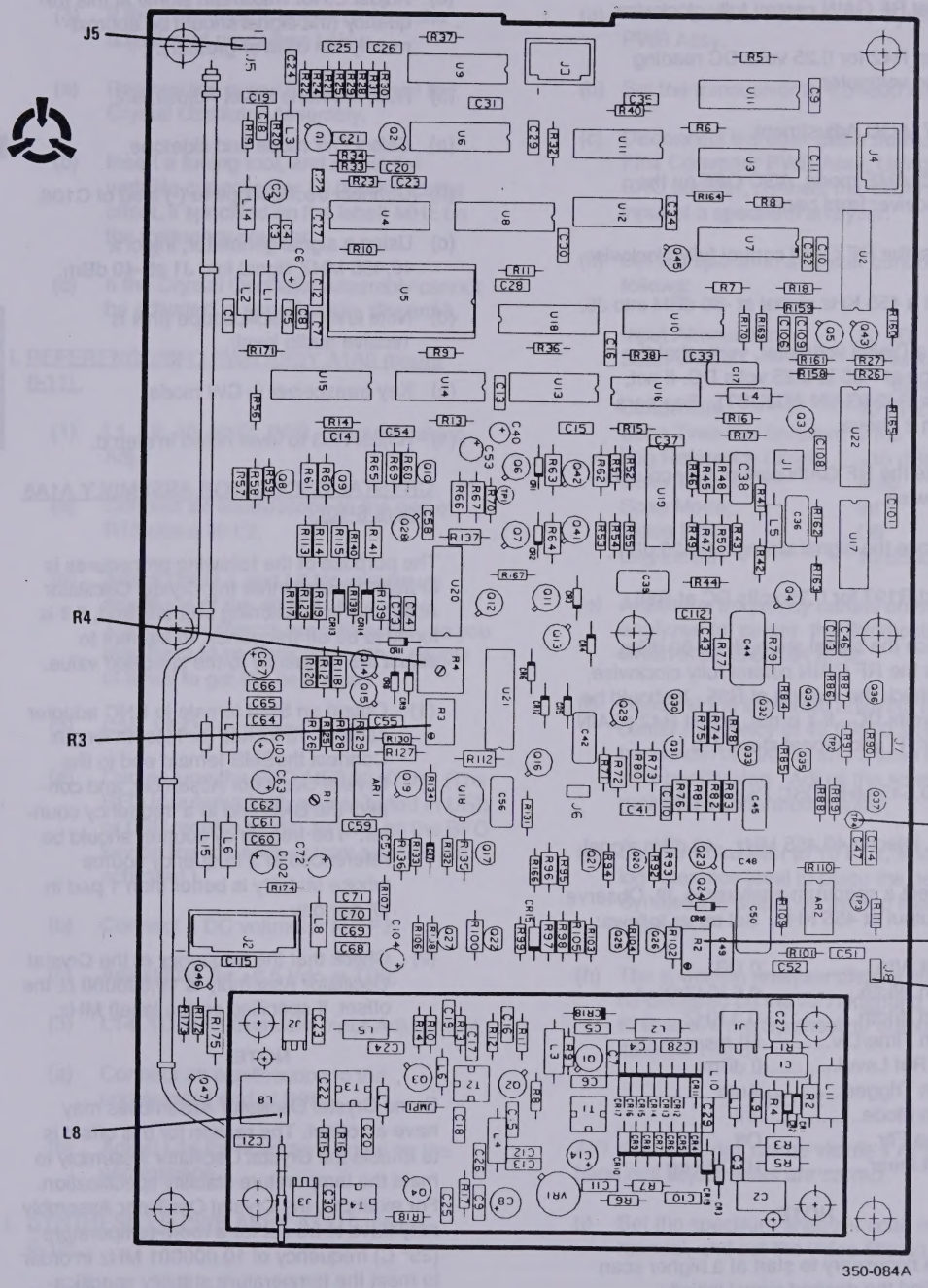


Figure 6-12. Synthesizer PWB Assy.

(d) Adjust RF GAIN control fully clockwise.

(e) Adjust R42 for 0.25 volts DC reading on the voltmeter.

(3) R197, AGC Adjustment.

(a) Select AME mode, AGC OFF on the transceiver front panel.

(b) Adjust the RF GAIN control fully clockwise.

(c) Inject a 455 KHz signal at -80 dBM into J5.

(d) With a Digital voltmeter, verify that the voltage at R85 is 0.25 volts DC. If not, adjust R42 (GAIN ADJUST). See paragraph 2 above.

(e) Rotate the RF GAIN control fully counter-clockwise.

(f) Increase the signal strength to -20 dBm.

(g) Adjust R197 for 0.25 volts DC at R85.

(h) Reduce the signal strength to -80 dBm, rotate the RF GAIN control fully clockwise, and check the voltage at R85. It should be 0.25 volts DC. If it is not, adjust R42 (GAIN ADJUST) and repeat steps e-h.

(4) L6, 39.545 MHZ OSC PeakIng Adj.

(a) At J1, inject a 40.455 MHz, -40 dBm signal.

(b) Connect a spectrum analyzer to J2. Observe the output at 455 KHz. Set up as follows:

- Input Attn .....0 DB
- Scan Width.....0.5 KHZ/Div.*
- Band Width.....0.3 KHZ
- Scan Time/Div.....50 msec
- Log Ref Level.....0 dBm
- Scan Trigger.....Auto
- Scan Mode.....Int
- Video Fltr.....Off
- Log/Linear.....10 DB Log

NOTE

It may be necessary to start at a higher scan width to find the desired signal initially.

(c) Adjust L6 for maximum signal at this frequency (the signal should be approximately -34 dBm or greater).

(5) R93, Sidetone Level Adjustment.

(a) Select CW mode and sidetone.

(b) Connect oscilloscope to (-) lead of C106.

(c) Using a signal generator, inject a 40.455 MHZ signal into J1 at -40 dBm.

(d) Note level of oscilloscope (this is receive audio level).

(e) Key transceiver in CW mode.

(f) Adjust R93 to level noted in step d.

h. CRYSTAL OSCILLATOR ASSEMBLY A1A8 (figure 6-10).

The purpose of the following procedures is to determine whether the Crystal Oscillator Assembly is functioning properly and, if it is found to be off-frequency, to attempt to adjust the frequency to the specified value.

(1) Obtain an SMB female to BNC adapter cable of 18 inches (or less) in length. Connect theSMB female end to the Crystal Oscillator Assembly, and connect the BNC end to a frequency counter. The frequency counter should be referenced to a frequency source whose stability is better than 1 part in 10^8 per day.

(2) Check that the frequency of the Crystal Oscillator Assembly is 10.000000 (± the offset, if specified on the label) MHz.

NOTE

Some Crystal Oscillator Assemblies may have an offset. The reason for this offset is to enable the Crystal Oscillator Assembly to meet the temperature stability specification. For example, the Crystal Oscillator Assembly may have to be set for a room-temperature (25° C) frequency of 10.000001 MHz in order to meet the temperature stability specification. In this case, the offset would be +1 Hz.

(3) If the frequency is not correct, do the adjustment procedure below.

(a) Remove the screw from the top of the Crystal Oscillator Assembly.

(b) Insert a tuning tool, and adjust the variable capacitor for 10.000000 (± the offset, if specified on the label) MHz on the frequency counter.

(c) If the Crystal Oscillator Assembly cannot be adjusted to specification, discard it.

i. REFERENCE/BFO PWB ASSY A1A9 (figure 6-11).

(1) L1, L2, 40 MHZ PER Output Peaking Adj.

(a) Connect an oscilloscope to the end of R15 closer to L2.

(b) Adjust both L1 and L2 for maximum amplitude of the 40 MHz sine wave. These adjustments are interactive, so you may have to go back and forth a couple of times to get the best result.

(2) C35, VCO Frequency Adjust:

(a) Center-tune the BFO (455.00 KHz). (The BFO is automatically center-tuned in USB or LSB receive mode, as long as the BFO key on the transceiver front panel is not activated.)

(b) Connect a DC voltmeter to TP2.

(c) Adjust C35 for +6.5 Vdc at TP2.

(3) L14, 1O MHz Standard Input Adjustment.

(a) Connect an oscilloscope to the ungrounded end of R99.

(b) Adjust L14 for maximum signal on the oscilloscope.

j. SYNTHESIZER PWB ASSY A1A10 (figure 6-12).

(1) RI, R3, R4: API Alignment Procedure.

(a) Remove the cover from the Synthesizer PWB Assy.

(b) Set the transceiver to 4.54800 MHz USB.

(c) Disconnect the coax cable from J5 on the First Converter PWB Assy. Using an SMB to BNC adapter, connect this cable to the RF input of a spectrum analyzer.

(d) Set the spectrum analyzer controls as follows:

Input Attenuation:	20 dB
Scan Width:	.05 MHz per division
Bandwidth:	10 KHz
Scan Time Per Division:	2 ms
Log Reference Level:	+10 dBm
Scan Trigger:	Auto
Scan Mode:	Int
Video Filter:	Off
Log/Linear:	10 dB log

(e) Adjust the frequency control on the spectrum analyzer to center the Synthesizer output, which is at 45.00304 MHz.

(f) Readjust the spectrum analyzer to give a center frequency of 45.00600 MHz with a bandwidth of 100 Hz and a scan width of 1 KHz per division. Adjust the scan time to maintain a calibrated display.

(g) Set the video filter to 10 KHz, and adjust the log reference level to place the peak of the Synthesizer output on the top line of the display.

(h) The spectrum analyzer display should now be centered on the API sideband, which is 3 KHz above the Synthesizer output at 45.00300 MHz.

NOTE

API sideband may not be visible if API sideband null adjustments are correct.

(i) Set the spectrum analyzer scan mode to manual, and set the video filter to 10 Hz.

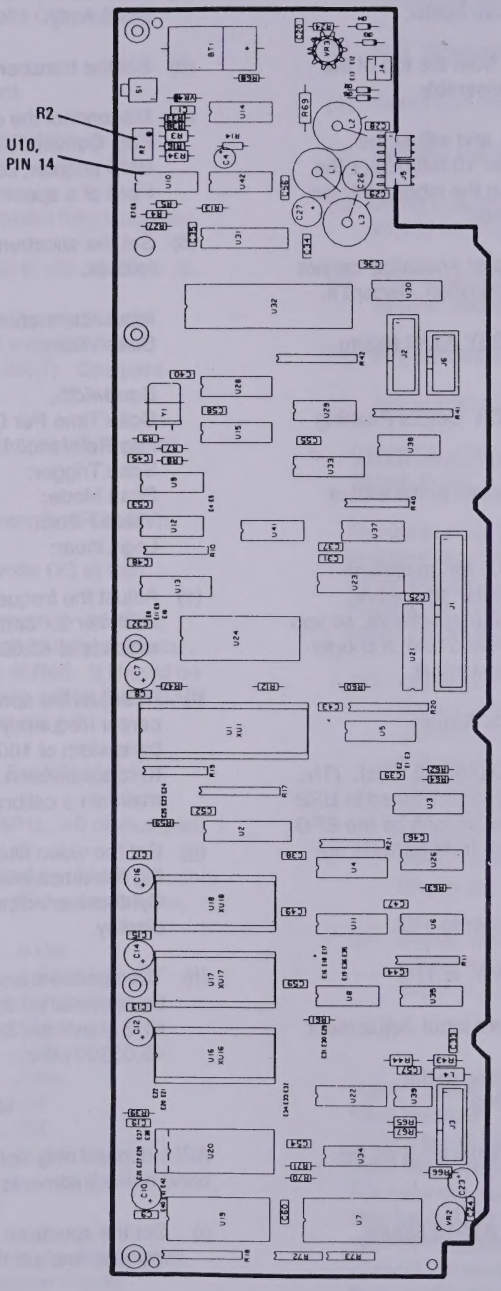


Figure 6-13. Transceiver Control PWB Assy.

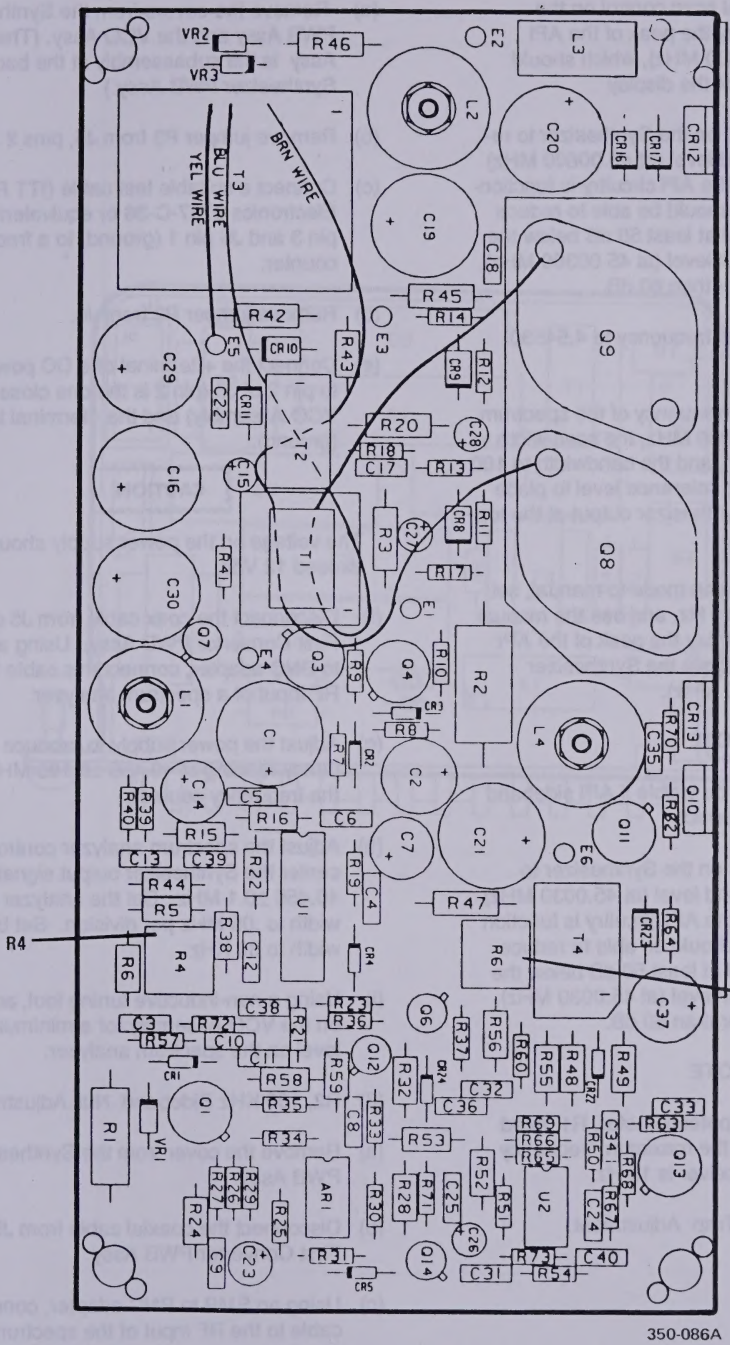


Figure 6-14. Multivoltage Supply PWB Assy.

(j) Adjust the manual scan control on the analyzer to display the peak of the API sideband (45.00600 MHz), which should be at the center of the display

(k) Adjust trim pot R3 on the Synthesizer to reduce the sideband level (at 45.00600 MHz) to a minimum. If the API circuitry is functioning properly, you should be able to reduce the sideband level at least 50 dB below the Synthesizer output level (at 45.00300 MHz), and typically better than 60 dB.

(l) Set the transceiver frequency to 4.54530 MHz.

(m) Adjust the center frequency of the spectrum analyzer to 45.00000 MHz, the scan width to 1 KHz per division, and the bandwidth to 100 Hz. Adjust the log reference level to place the peak of the Synthesizer output at the top line of the display.

(n) Set the analyzer scan mode to manual, set the video filter to 10 Hz, and use the manual scan control to display the peak of the API sideband 3 KHz above the Synthesizer output (at 45.0030 MHz).

NOTE

API sideband may not be visible if API sideband null adjustments are correct.

(o) Adjust trim pot R4 on the Synthesizer to reduce the sideband level (at 45.0030 MHz) to a minimum. If the API circuitry is function ing properly, you should be able to reduce the sideband level at least 50 dB below the Synthesizer output level (at 45.0030 MHz), and typically better than 60 dB.

NOTE

The API 4 adjustment potentiometer, R1, need not be adjusted, since the maximum frequency resolution of the transceiver is 10 Hz.

(2) L8, 40.455 MHz Trap Adjustment.

(a) Remove the covers from the Synthesizer PWB Assy and the VCO Assy. (The VCO Assy is the subassembly at the back of the Synthesizer PWB Assy.)

(b) Remove jumper P3 from J5, pins 2 and 3.

(c) Connect a suitable test cable (ITT Pomona Electronics 3787-C-36 or equivalent) from J5 pin 3 and J5 pin 1 (ground) to a frequency counter.

(d) Remove jumper P2 from J8.

(e) Connect the + terminal of a DC power supply to pin 2 of J8 (pin 2 is the one closer to the VCO Assembly) and the - terminal to TP4 (ground).

CAUTION

The voltage on the power supply should not exceed 12 Vdc.

(f) Disconnect the coax cable from J5 on the First Converter PWB Assy. Using an SMB to BNC adapter, connect this cable to the RF input of a spectrum analyzer.

(g) Adjust the power supply to produce a frequency reading of 40.455 ±0.100 MHz on the frequency counter.

(h) Adjust the spectrum analyzer controls to center the Synthesizer output signal at 40.455 ±0.1 MHz. Set the analyzer scan width to .05 MHz per division. Set bandwidth to 30 KHz.

(i) Using a non-inductive tuning tool, adjust L8 on the VCO Assembly for a minimum signal level on the spectrum analyzer.

(3) R2, 100 KHz Sideband Null Adjustment

(a) Remove the cover from the Synthesizer PWB Assy.

(b) Disconnect the coaxial cable from J5 on the First Converter PWB Assy.

(c) Using an SMB to BNC adapter, connect this cable to the RF input of the spectrum analyzer.

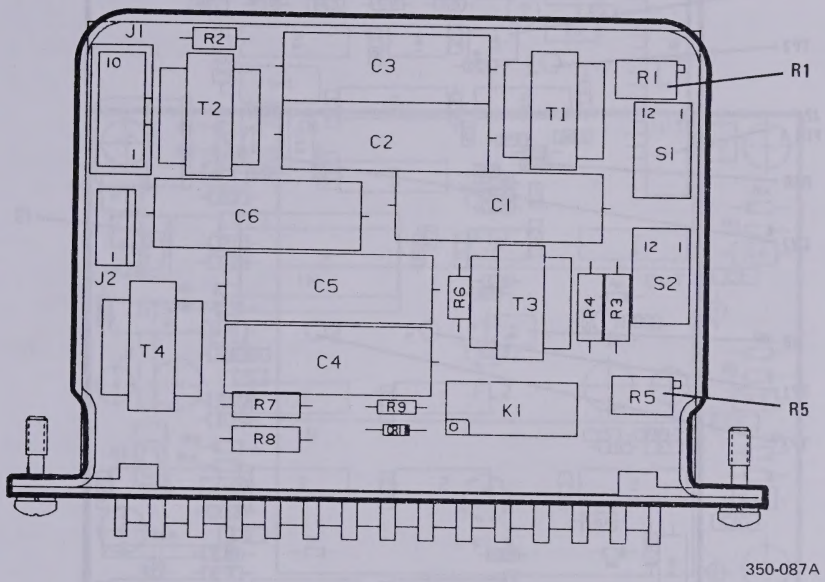


Figure 6-15. Audio Interface PWB Assy.

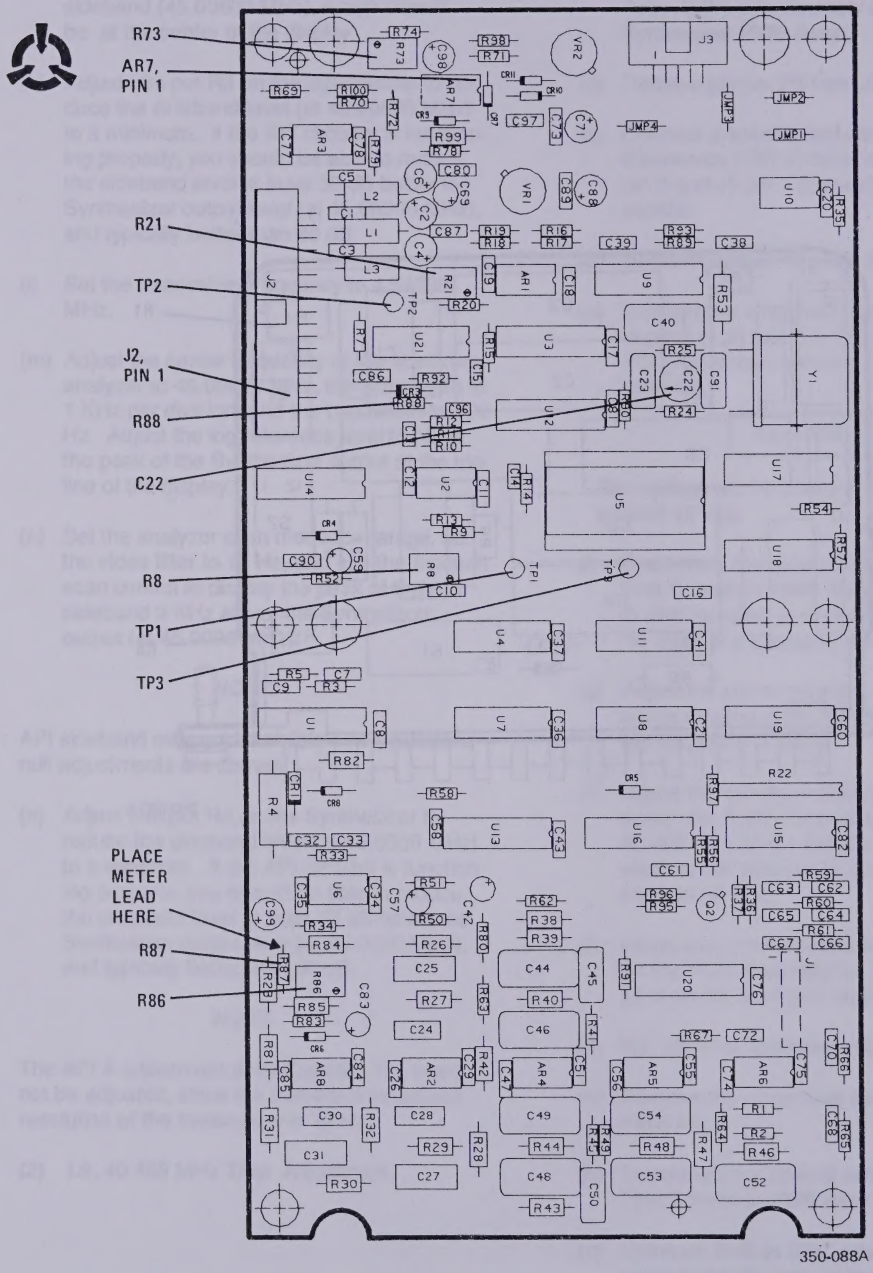


Figure 6-16. AFSK Keyer/Converter PWB Assy.

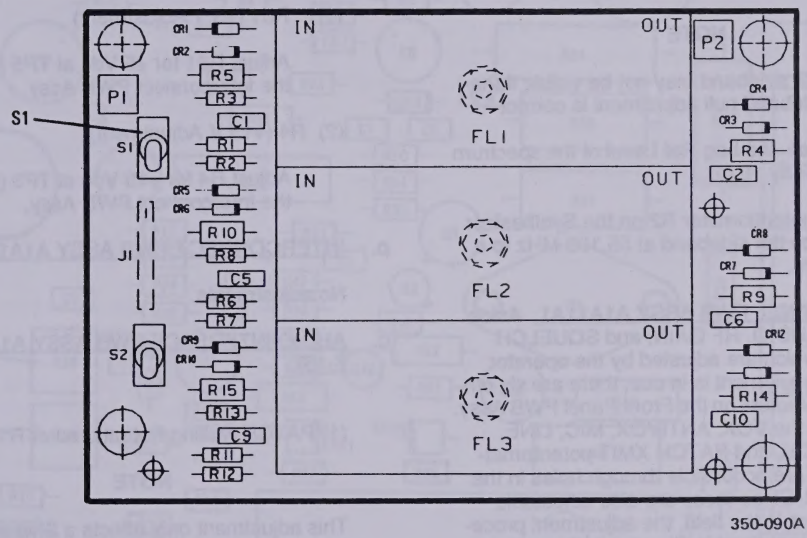


Figure 6-17. AFSK IF Filter PWB Assy.

(d) Set the transceiver to 14.54500 MHz USB.

(e) Adjust the spectrum analyzer to center the Synthesizer output at 55.000 MHz on the analyzer display.

(f) Set the input attenuation on the spectrum analyzer to 20 dB.

(g) Adjust the Log Ref Level controls to place the peak of the Synthesizer signal (55.000 MHz) a the top line of the analyzer display (0 dB line).

(h) Retune the center frequency of the spectrum analyzer to 55.100 MHz. The Synthesizer sideband at 55.100 MHz should now be displayed.

NOTE

The 100 KHZ sideband may not be visible if the 100 KHZ sideband null adjustment is correct

(i) Decrease the Log Ref Level of the spectrum analyzer by 10 dB.

(j) Adjust potentiometer R2 on the Synthesizer to reduce the sideband at 55.100 MHz to a minimum.

k. FRONT PANEL PWB ASSY A1A11A1. Aside from the AUDIO, RF GAIN, and SQUELCH controls, which are adjusted by the operator while the equipment is in use, there are six other potentiometers on the Front Panel PWB Assy. These are the VOX, ANTIVOX, MIC, LINE, PATCH RCV, and PATCH XMIT potentometers, which are accessible through holes in the front panel. Since these are also adjustable by operators in the field, the adjustment procedures are contained in Chapter 4, Operation.

l. DISPLAY ASSEMBLY A1A11A2.

No adjustments.

m. TRANSCEIVER CONTROL PWB ASSY A1A12 (figure 6-13).

Power Off Reset Potentiometer R2 Adjustment

(a) Measure the +13.6 Vdc supply line at TP4 (yellow) on the Interconnect PWB Assy with a multimeter. Note the actual voltage.

(b) Monitor the dc voltage at U10 pin 14 on the Transceiver Control PWB Assy with a multimeter.

(c) Adjust R2 to produce a dc voltage at U10 pin14 which is 0.56 times the voltage measured at TP4 on the Interconnect PWB Assy.

n. LPA/COUPLER INTERFACE PWB ASSY A1A13.

No adjustments.

o. MULTIVOLTAGE SUPPLY ASSY A1A14 (figure 6-14).

(1) R61 (+5 V Adjustment)

Adjust R61 for +5 Vdc at TP5 (green) on the Interconnect PWB Assy.

(2) R4 (+15 V Adjustment)

Adjust R4 for +15 Vdc at TP3 (orange) on the Interconnect PWB Assy.

p. INTERCONNECT PWB ASSY A1A15.

No adjustments.

q. AUDIO INTERFACE PWB ASSY A1A16 (figure 6-15).

(1) PATCH Nulling Potentiometer R1

NOTE

This adjustment only affects a 2-wire PATCH hookup.

(a) Set the PATCH selector switch (S1) on the Audio Interface PWB Assy to the "2" position.

(b) Connect the nominal 600-ohm system termination across the "2W" PATCH terminals on TB1 at the rear of the transceiver.

(c) Set the transceiver to receive USB mode at 2.4560 MHz.

(d) Activate the BIT test tone by placing the jumper plug (PN 65474-001, FSCM 00779) at J7 on the Low Pass Filter PWB Assy to the test position (between pins 2 and 3).

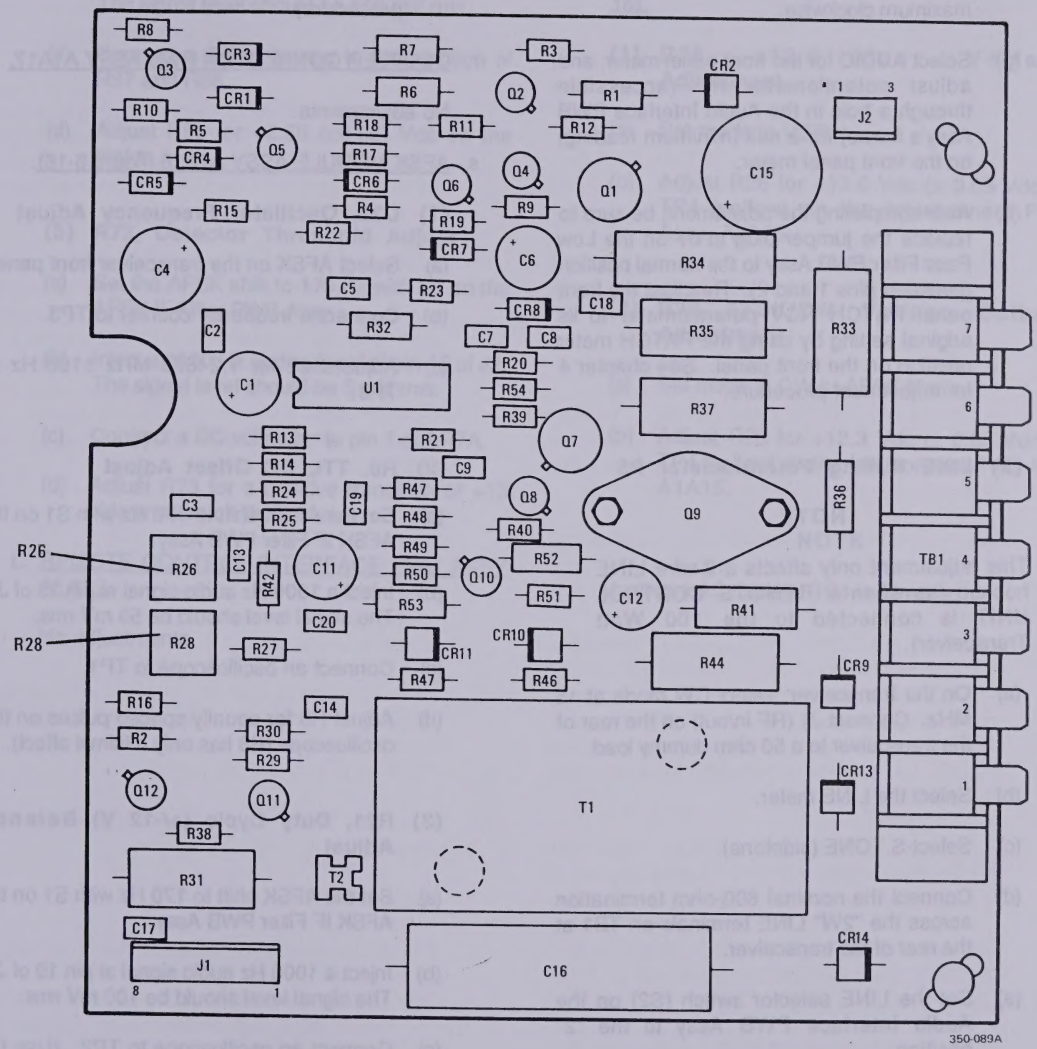


Figure 6-18. 13.6 Vdc Power Supply PWB Assy.

(e) Listen for an audio tone from the speaker.

(f) Select PATCH for the audio source, and select PATCH for the meter. Note the output level. Temporarily adjust the PATCH RCV potentiometer on the front panel to maximum clockwise.

(g) Select AUDIO for the front panel meter, and adjust potentiometer R1 (accessible through a hole in the Audio Interface PWB Assy's frame) for a null (minimum reading) on the front panel meter.

(h) After completing the adjustment, be sure to replace the jumper plug at J7 on the Low Pass Filter PWB Assy to the normal position (between pins 1 and 2). Readjust the front panel PATCH RCV potentiometer to its original setting by using the PATCH meter position on the front panel. See chapter 4 for adjustment procedure.

(2) LINE Nulling Potentiometer R5

NOTE

This adjustment only affects a 2-wire LINE hookup (as when a REMOTE CONTROL UNIT is connected to the 100 Watt Transceiver).

(a) On the transceiver, select CW mode at 15 MHz. Connect J1 (RF in/out) on the rear of the transceiver to a 50 ohm dummy load.

(b) Select the LINE meter.

(c) Select S TONE (sidetone).

(d) Connect the nominal 600-ohm termination across the "2W" LINE terminals on TB1 at the rear of the transceiver.

(e) Set the LINE selector switch (S2) on the Audio Interface PWB Assy to the "2" position.

(f) Adjust the LINE potentiometer on the front panel of the transceiver fully clockwise.

(g) Key the transceiver with the CW key , and adjust R5 (accessible through a hole in the chassis frame and the Audio Interface PWB Assy's frame) for a null (minimum reading) on the meter.

(h) Rotate the LINE potentiometer to its former position (see Chapter 4 for the adjustment procedure).

r. COUPLER CONNECTOR PWB ASSY A1A17.

No adjustments.

s. AFSK MODULE ASSY A1A18 (figure 6-16).

(1) C22, Oscillator Frequency Adjust

(a) Select AFSK on the transceiver front panel.

(b) Connect a frequency counter to TP3.

(c) Adjust C22 for 1.24890 MHz ±100 Hz at TP3.

(2) R8, TTL DC Offset Adjust

(a) Set the AFSK shift to 170 Hz with S1 on the AFSK IF Filter PWB Assy.

(b) Inject a 1000 Hz audio signal at pin 19 of J2. The signal level should be 50 mV rms.

(c) Connect an oscilloscope to TP1.

(d) Adjust R8 for equally spaced pulses on the oscilloscope (R8 has only minimal affect).

(3) R21, Duty Cycle (+/-12 V) Balance Adjust

(a) Set the AFSK shift to 170 Hz with S1 on the AFSK IF Filter PWB Assy.

(b) Inject a 1000 Hz audio signal at pin 19 of J2. The signal level should be 100 mV rms.

(c) Connect an oscilloscope to TP2. (Use the DC coupled input to the oscilloscope.)

(d) Adjust R21 so that the signal at TP2 is a symmetrical signal approximately ± 12 Vdc relative to ground at twice the audio input frequency.

(4) R86, AFSK Meter Balance Adjust

(a) Set the AFSK shift to 170 Hz with S1 on the AFSK IF Filter PWB Assy.

(b) Inject a 1000 Hz audio signal at pin 19 of J2. The signal level should be 100 mV rms.

(c) Connect a DC voltmeter to the junction of R87 and R88.

(d) Adjust R86 for +2.50 (±0.05) Vdc on the meter.

(5) R73, Detector Threshold Adjust

(a) Set the AFSK shift to 170 Hz with S1 on the AFSK IF Filter PWB Assy.

(b) Inject a 1000 Hz audio signal at pin 19 of J2. The signal level should be 5 mV rms.

(c) Connect a DC voltmeter to pin 1 of AR7A.

(d) Adjust R73 for a positive transition of +13 Vdc or more on the meter.

t. REMOTE CONTROL INTERFACE PWB ASSY A1A19.

No adjustments.

u. POWER SUPPLY PROTECTION AND CONTROL PWB ASSY A2A1.

No adjustments.

v. 13.6 V POWER SUPPLY ASSY A2A2 (figure 6-18).

(1) R26, +13.6 Vdc Voltage Adjustment.

(a) Set mode to USB.

(b) Adjust R26 for +13.6 Vdc (± 0.05 Vdc) at TP4 (yellow) on the Interconnect PWB Assy, A1A15.

(2) R28, AFSK/CW Voltage Cutback Adjustment

(a) Set mode at CW or AFSK Mode.

(b) Adjust R28 for +12.3 Vdc (± 0.05 Vdc) at TP4 (yellow) on the Interconnect PWB Assy A1A15.

NOTE

Maximum AC ripple at TP4 is 50 mVac.

APPENDIX

CHECKS PERFORMED DURING AUTOMATIC BIT ROUTINES FOR THE TRANSCEIVER

1. Turns on all front panel indicators for the duration of the test for inspection by the operator.

2. Checks for major modules present by testing the ability to send data to and receive data from modules.

3. Remote Control Interface PWB Assy (A1A19) - If installed, checks UART loopback and baud rate switch.

4. Multivoltage Supply Assy (A1A14) - Checks +15V and -15V output voltages and compares them with stored limits.

5. Disables speaker and mutes 600-ohm line.

6. Reference/BFO PWB Assy (A1A9) - Verifies the presence of all outputs and verifies frequency lock of BFO at both ends of the frequency range.

7. Synthesizer PWB Assy (A1A10) - Verifies the presence of output and frequency lock at both ends of the tuning range.

8. Low Pass Filter PWB Assy (A1A5) - Activates BIT Oscillator and checks receive RF output with all filters deselected, then checks output with each filter selected in turn. If all filters pass, rechecks with all filters deselected, then selects Band 6, and sets the synthesizer to receive the BIT Oscillator.

9. First Converter PWB Assy (A1A3) - Activates BIT Oscillator signal and verifies the presence of Rx (receive) IF output.

10. Receiver PWB Assy (A1A7) - Activates BIT Oscillator and verifies the presence of IF to filters.

11. IF Filter PWB Assy (A1A2) - Activates BIT Oscillator, then selects each filter, using the Synthesizer to center the BIT signal in each passband, and verifies the presence of 455 KHz IF output. If an AFSK option is installed, these filters are checked in a similar manner.

12. Receiver PWB Assy (A1A7) - Bypasses volume and squelch controls, sets RF gain at maximum, and verifies that there is no line audio in USB. Activates BIT Oscillator and verifies the presence of a line audio level.

13. AGC/TGC PWB Assy (A1A6) - Checks signal strength in USB at maximum RF gain with and without the BIT Oscillator activated. Checks signal strength with the BIT Oscillator activated at minimum RF gain.

14. AFSK - Checks for presence of module; if present, keys module, places it in a loopback configuration, and verifies that a mark and space applied to the keyer are detected as a mark and space by the converter. If receive-only testing has been initiated, the test stops and the current operating status is restored. If receive/transmit testing has been initiated, the following additional steps occur.

NOTE

The transceiver must be connected to a load with a VSWR of 2.0 to 1 maximum in order for this portion of the routine to proceed to completion.

15. Exciter PWB Assy (A1A1) - Applies a 1 KHz test signal to the MIC input, selects USB mode, and keys the transmitter; verifies the presence of 455 KHz IF output from Exciter.

16. Receiver PWB Assy (A1A7) - Verifies the presence of IF to filters.

17. Exciter PWB Assy (A1A1) -

    (a) Verifies the presence of Exciter IF output;

    (b) disables the 1 KHz test signal, selects AME, and verifies the presence of Exciter IF output; and (c) selects CW mode and verifies the presence of Exciter IF output.

18. First Converter PWB Assy (A1A3) - Keys the radio in CW and verifies the presence of Tx (transmit) RF output.

19. 100 Watt PA (A1A4) - Keys the transmitter in CW and verifies the presence of Tx RF output.

20. Low Pass Filter PWB Assy (A1A5) - Keys the transmitter in CW and verifies the presence of the signal at RF IN/OUT.

21. AGC/TGC PWB Assy (A1A6) - Keys the transmitter in CW. Verifies the correct transceiver output power level and verifies that the TGC system has stabilized at a normal control level.

22. Restores the radio to the current operating status.

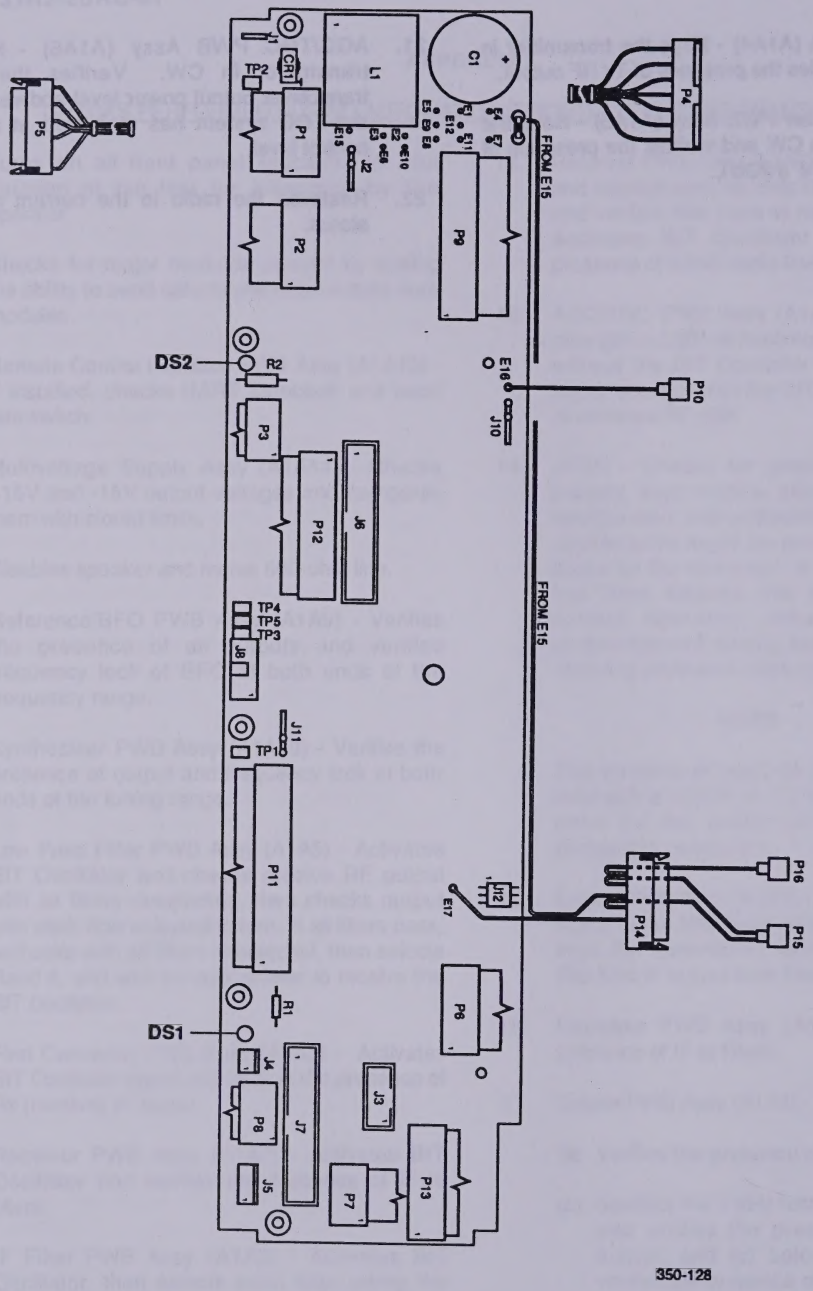


Figure 6-19. Interconnect PWB Assy. A1A15

CHAPTER 7

ILLUSTRATED PARTS BREAKDOWN

Section I. INTRODUCTION

7-1. PURPOSE. This chapter lists, illustrates, and describes the assemblies and detail parts for the 100 Watt Transceiver. Its purpose is for the identification, requisitioning, and issuance of parts at the organizational (on-equipment) level.

7-2. SCOPE. Only parts that are coded as replaceable at the organizational level are listed in this chapter. These include the major assemblies and a few detail parts. Mounting hardware is listed only if it is used to attach a replaceable assembly or part and only if it is not held captive to the assembly or part. In general, the assemblies and parts installed at the time the 100 Watt Transceiver was manufactured are listed and identified in this chapter. When an assembly or part (including vendor items), which is different from the original, was installed during the manufacture of later items, series or blocks, all assemblies and parts are listed (and "Usable-On" coded). However, when the original assembly or part does not have continued application (no spares of the original were procured or such spares are no longer authorized for replacement), only the preferred assembly or part is listed. Also, when an assembly or part was installed during modification, and the original does not have continued application, only the preferred item is listed. Interchangeable and substitute assemblies and parts, subsequently authorized by the Government, are not listed in this chapter; such items are identified by information available through the Interchangeable and Substitute (I & S) Data Systems. Refer to T.O. 00-25-184. When a standard size part can be replaced with an oversize or undersize part, the latter parts, showing sizes, are also listed. Repair Parts Kits and Quick Change Units are listed when they are available for replacement.

7-3. CHAPTER ORGANIZATION. This chapter is divided into two sections. Section I, INTRODUCTION, explains the purpose, scope, and organization of the chapter. Section II, MAINTENANCE PARTS LIST, consists of illustrations, in which the assemblies and detail parts of the 100 Watt Transceiver are identified by numbers (called index numbers), followed by a list which contains parts numbers, descriptions, and other relevant data for the items identified on the illustrations.

7-4. SOURCE, MAINTENANCE, AND RECOVERABILITY (SMR) CODES. This chapter contains Air Force Peculiar In-Being Source and Repair Codes only. Definitions of these SMR codes, as well as detailed coding criteria and transposition matrices for each coding method may be obtained from T.O. 00-25-195. Refer to page 7-3.

7-5. FEDERAL SUPPLY CODES FOR MANUFACTURERS (FSCM). The codes used in this chapter are as follows. The first list is in numerical order by FSCM; the second is in alphabetical order by manufacturer name.

FSCM	NAME AND ADDRESS
00141	PIC Design Corporation Benson Road P. O. Box 1004 Middlebury, Connecticut 06762
00779	Amp Incorporated 2800 Fulling Mill P. O. Box 3508 Harrisburg, Pennsylvania 17105
06402	E-T-A Circuit Breakers 7400 North Croname Road Chicago, Illinois 60648
06540	Mite Corporation Amatom Electronic Hardware Division 446 Blake Street New Haven, Connecticut 06515
08041	Robertshaw Controls Company Industrial Instrument Division 333 North Euclid Way P. O. Box 3775 Anaheim, California 92803
08484	Breeze-Eastern Corporation Subsidiary of Transtechnology Corp. 700 Liberty Avenue Union, New Jersey 07083
09353	C and K Components Incorporated 15 Riverdale Avenue Newton, Massachusetts 02158
14304	Harris Corporation RF Communications Group 1608 University Avenue Rochester, New York 14610
15330	General Connector Corporation Subsidiary of the Union Corporation 80 Bridge Street Newton, Massachusetts 02158
18876	Dept. of U. S. Army Missile Command Redstone Arsenal, Alabama 35809
28482	Electronic Laboratory Supply Co. 7208 Germantown Avenue Philadelphia, Pennsylvania 19119
70485	Atlantic India Rubber Works Incorporated 571 West Polk Street Chicago, Illinois 60607
71400	Bussman Division of McGraw-Edison Company 114 Old State Road P. O. Box 14460 St. Louis, Missouri 63178
71468	ITT Cannon Electric Division of ITT Corporation 10550 Talbert Avenue P. O. Box 8040 Fountain Valley, California 92708
74199	Quam Nichols Company 218 East Marquette Road Chicago, Illinois 60637
77342	AMF Incorporated Potter and Brumfield Division 200 Richland Creek Drive Princeton, Indiana 47671
80031	Mepco/Electra Inc. 22 Columbia Road Morristown, N. J. 07960
81349	Military Specification Code
82877	Rotron Incorporated Custom Division 7 Hasbrouck Lane Woodstock, New York 12498
83014	Hartwell Corporation 900 South Richfield Road Placentia, California 92670
86797	Rogan Corporation 3455 Woodhead Drive Northbrook, Illinois 60062
88044	Aeronautical Standards Group Department of the Navy and Air Force
94033	Lapointe Industries Inc. Electronic Products Division 155 West Main Street Rockville, Connecticut 06066
95146	Alco Electronic Products Incorporated 1551 Osgood Street North Andover, Massachusetts 01845
96906	Military Specification Code

NAME AND ADDRESS	FSCM
Alco Electronic Products Incorporated 1551 Osgood Street North Andover, Massachusetts 01845	95146
AMF Incorporated Potter and Brumfield Division 200 Richland Creek Drive Princeton, Indiana 47671	77342
Amp Incorporated 2800 Fulling Mill P. O. Box 3508 Harrisburg, Pennsylvania 17105	00779
Atlantic India Rubber Works Incorporated 571 West Polk Street Chicago, Illinois 60607	70485
Breeze-Eastern Corporation Subsidiary of Transtechnology Corp. 700 Liberty Avenue Union, New Jersey 07083	08484
Bussman Division of McGraw-Edison Company 114 Old State Road P. O. Box 14460 St. Louis, Missouri 63178	71400
C and K Components Incorporated 15 Riverdale Avenue Newton, Massachusetts 02158	09353
Electronic Laboratory Supply Co. 7208 Germantown Avenue Philadelphia, Pennsylvania 19119	28482
E-T-A Circuit Breakers 7400 North Croname Road Chicago, Illinois 60648	06402
General Connector Corporation Subsidiary of the Union Corporation 80 Bridge Street Newton, Massachusetts 02158	25330
Harris Corporation RF Communications Group 1680 University Avenue Rochester, New York 14610	14304
Hartwell Corporation 900 South Richfield Road Placentia, California 92670	83014
ITT Cannon Electric Division of ITT Corporation 10550 Talbert Avenue P. O. Box 8040 Fountain Valley, California 92708	71468
Lapointe Industries Inc. Electronic Products Division 155 West Main Street Rockville, Connecticut 06066	94033
Mepco/Electra Inc. 22 Columbia Road Morristown, New Jersey 07960	80031
Mite Corporation Amatom Electronic Hardware Division 446 Blake Street New Haven, Connecticut 06515	06540
PIC Design Corporation Benson Road P. O. Box 1004 Middlebury, Connecticut 06762	00141
Quam Nichols Company 218 East Marquette Road Chicago, Illinois 60637	74199
Robertshaw Controls Company Industrial Instrument Division 333 North Euclid Way P. O. Box 3775 Anaheim, California 92803	08041
Rogan Corporation 3455 Woodhead Drive Northbrook, Illinois 60062	86797
Rotron Incorporated Custom Division 7 Hasbrouck Lane Woodstock, New York 12498	82877

Note: Field and organizational maintenance of the modules and circuit card assemblies is limited only to the removals, replacements, and alignments given in chapter 6.

JOINT MILITARY SERVICES UNIFORM SMR CODING MATRIX T.O. 00-25-195

SOURCE				MAINTENANCE USE		MAINTENANCE REPAIR		RECOVERABILITY		ERRC CODE	
1st Position		2nd Position		3rd Position		4th Position		5th Position		6th Position	
P	Procurable	A	Stocked	O	Remove/ Replace at Organizational Level	Z	No Repair	Z	Nonreparable Condemn at 3rd Position Level	N	Nonrecoverable XB3 Condemn at Any Level
		B	Insurance								
		C	Deteriorative								
		E	Support Equipment, Stocked								
		F	Support Equipment, Nonstocked			B	No Repair Recondition	O	Reparable Condemn at Organizational	P	Recoverable XF3 Condemn at Field
		G	Sustained Life Support							C	Recoverable XD1 (SCARS) Condemn at Depot
K	Component of a Repair Kit	F	Intermediate Kit	F	Remove/ Replace at Intermediate Level	O	Repair at Organizational	F	Reparable Condemn at Intermediate	T	Recoverable XD2 Condemn at Depot
		D	Depot Kit			F	Repair at Intermediate				
		B	In Both Kits								
M	Manufacture	O	Organization								
		F	Intermediate								
		D	Depot	D	Remove/Replace at Depot Level	D	Limited Repair at O or F Level Overhaul at Depot	D	Reparable Condemn at Depot	S	Nonexpendable Support Equipment, Depot ND2
A	Assemble	O	Organization								
		F	Intermediate								
		D	Depot								
X	Nonprocured	A	Requisition NHA			L	Repair at Depot	A	Special Handling	U	Nonexpendable Support Equipment, Organizational and Intermediate NF2
		B	Reclamation from IM								
		C	Mfg Drawings								

Section II. MAINTENANCE PARTS LIST

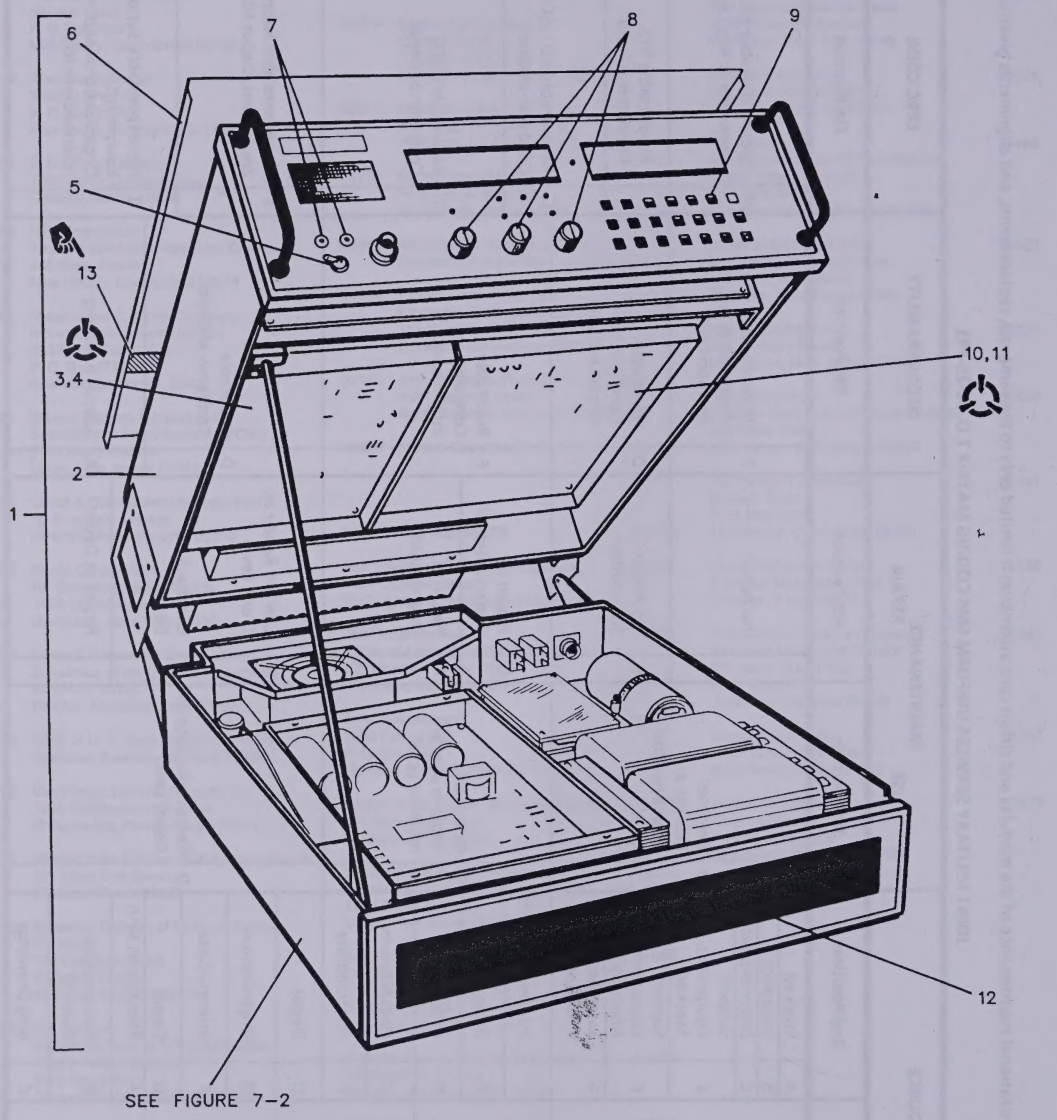


Figure 7-1. 100 Watt Transceiver, RT-1446/URC, Front View

FIGURE & INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
			ILLUSTRATED PARTS BREAKDOWN			
7-1-	10085-0000	14304	RCVR-XMTR, Radio*			PE0DD
1-	10085-0010	14304	. Transceiver Assy	1		XB
2-	10085-0100	14304	. Upper Chassis Assy, A1	1		XB
3-	10085-5200	14304	. Receiver PWB Assy, A1A7	1		PA0DD
4-	10085-5174	14304	. Cover, (for RCVR PWB)	1		XB
5-	7401T1ZGE	09353	. Switch, Toggle A1A11S1	1		PA0ZZ
6-	10085-0105	14304	. Cover, Top	1		XB
7-	66101-3	00779	. Socket, Elec	2		PA0ZZ
8-	MS-67-1-DC-WD	86797	. Knob	3		PA0ZZ
	AN565DC6L3	88044	. . Screw, Set (AP)	6		PA0ZZ
9-	10085-2007	14304	. Keypad, A1A11KP1	1		PA0ZZ
10-	10085-5400	14304	. Exciter PWB Assy, A1A1	1		PA0DD
11-	10085-5175	14304	. Cover (for Exciter PWB)	1		XB
12-	10085-0271	14304	. Filter, Air	1		PA0ZZ
-13	31-0064040	07700	Shielding Gasket Electronic	1		PA0ZZ

*Installation requires Ancillary Kit 10085-0060 (See Figure 7-9).

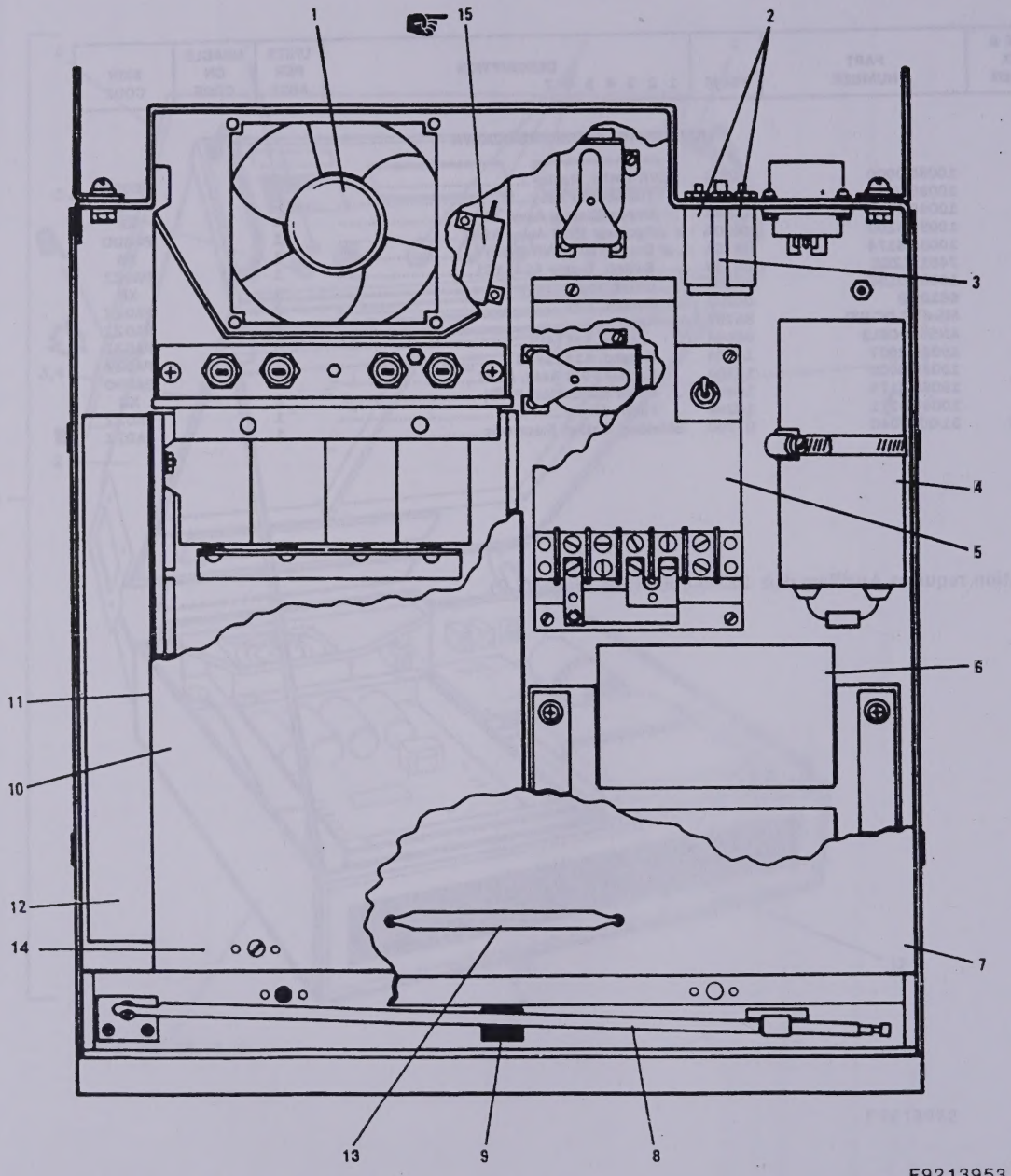


Figure 7-2. 100 Watt Transceiver, RT-1446/URC, Bottom Half

FIGURE & INDEX NUMBER	PART NUMBER	FSCM	DESCRIPTION 1 2 3 4 5 6 7	UNITS PER ASSY	USABLE ON CODE	SMR CODE
7-2-	10085-0200	14304	Cover Assembly, XCVR Power Supply	1		PAODD
-1	028868	82877	. Fan, A2B1	1		PAOZZ
	MS51957-38	96906	. Screw, Machine (AP)	4		PAOZZ
	MS15795-805	96906	. Washer, Flat (AP)	4		PAOZZ
-2	W58XB1A6A-6 A2CB1, A2CB2	77342	. Circuit Breaker,	2		PAOZZ
-3	41-3-S14-LN2-50	06402	. Circuit Breaker, A2CB3	1		PAOZZ
-4	C21-0006-663 A2C1	14304	. Capacitor, Fxd, Elctlt,	1		
	Z31-0005-006	14304	. Clamp, Hose (AP)	1		XB
-5	10085-0290 Assy, A2A1	14304	. PS Contrl/Protect PWB	1		PAODD
-6	10085-0213	14304	. Transformer, RF, A2T1	1		PAOZZ
	10085-0278	14304	. Bracket, Mtg (AP)	2		XB
	MS51958-72	96906	. Screw, Machine (AP)	4		PAOZZ
	MS15795-808	96906	. Washer, Flat (AP)	4		PAOZZ
-7	10085-0249	14304	. Cover, Power Supply	1		XB
	10029-0073	14304	. Handle	1		XB
	10085-0079	14304	. Label, HV Danger	1		XB
-8	10085-0257	14304	. Brace	1		XB
	10085-0273	14304	. Bracket, Angle (AP)	1		XB
	MS51957-16	96906	. Screw, Machine (AP)	2		PAOZZ
	MS15795-803	96906	. Washer, Flat (AP)	2		PAOZZ
	MS15795-807	96906	. Washer, Flat (AP)	2		PAOZZ
	4318	00141	. Screw, Machine (AP)	1		PAOZZ
-9	Z17-0004-004	14304	. Bumper	1		XB
-10	10085-0260	14304	. Power Supply Assy, A2A2	1		PAODD
-11	10085-0263	14304	. Cover, Power Supply	1		XB
	10085-5129	14304	. Label	1		XB
-12	10085-0240	14304	. EMI Filter Assy, A2A3	1		PAODD
-13	10029-0073	14304	. Peripheral Utility Lateral Lifting Transfer Action Booster	1		PAOZZ
-14	F4-30-SS	72794	Captive, Screw	2		PAZZN
-15	RER75F1R00R	81349	. Resistor, Fxd, WW,1 OHM	1		PAOZZ

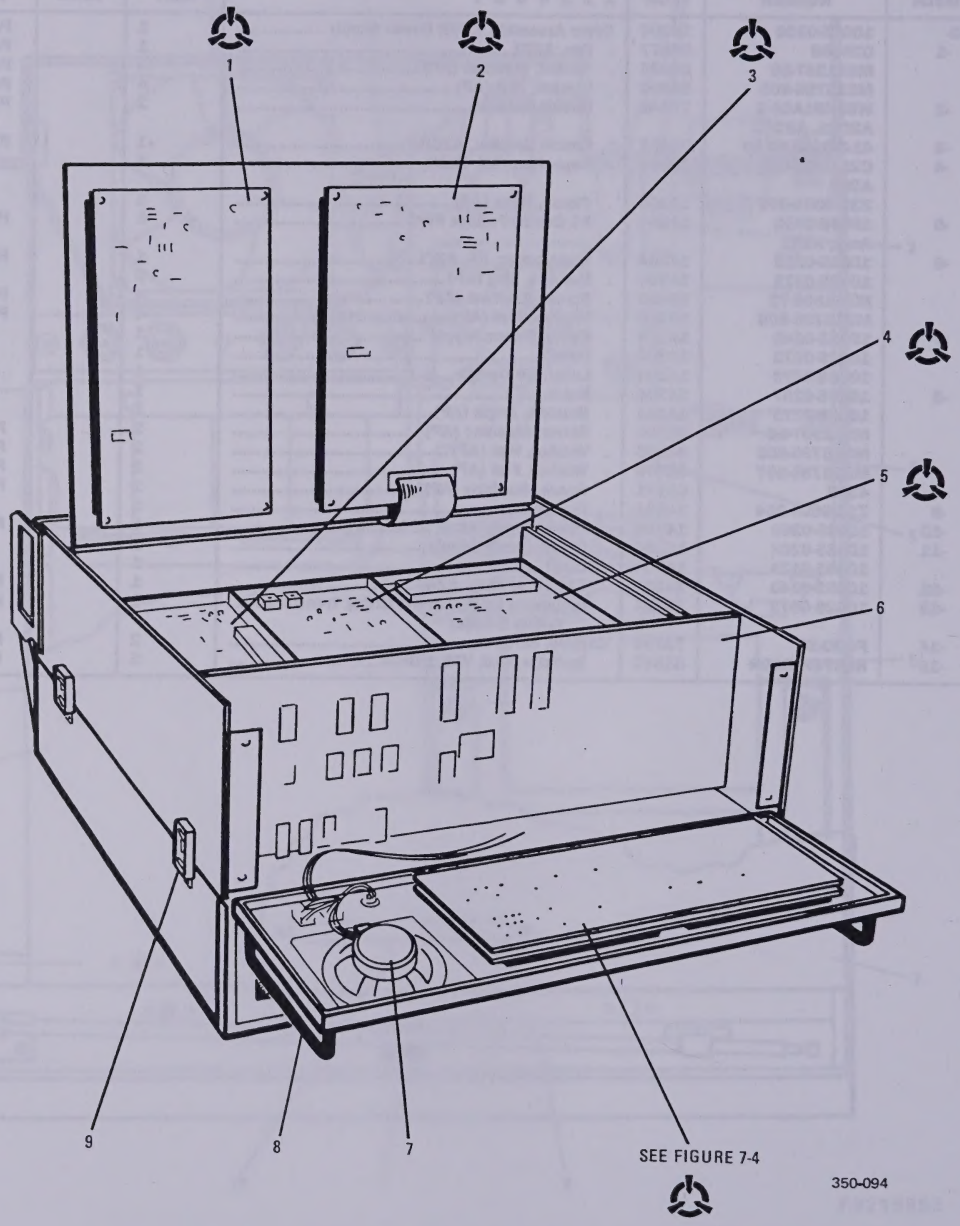


Figure 7-3. 100 Watt Transceiver, RT-1446/URC, Internal Components

ILLUSTRATED PARTS BREAKDOWN

Fig. & Index No.	Part No.	FSCM	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code	SMR Code
7-3- 1	10085-6000	14304	Module Assy, AFSK, A1A18 (Fig. 7-8)	1		PAODD
2	10085-5250	14304	AGC/TGC PWB Assy, A1A6	1		PAODD
3	10085-5000	14304	First Converter PWB Assy, A1A3	1		PAODD
	10085-5171	14304	Cover (for first Conv PWB)	1		XB
4	10085-5500	14304	REF/BFO PWB Assy, A1A9	1		PAODD
	10085-5172	14304	Cover (for REF/BFO PWB)	1		XB
5	10085-5600	14304	Synthesizer PWB Assy, A1A10	1		PAODD
	10085-5173	14304	Cover (for Synthesizer PWB)	1		XB
6	10085-9000	14304	XCVR Control PWB Assy, A1A12	1		PAODD
7	82-8666	74199	Speaker, A1A11LS1	1		PAOZZ
	MS51957-18	96906	Screw, Machine (AP)	2		PAOZZ
	MS15795-803	96906	Washer, Flat (AP)	2		PAOZZ
	H-6769	96906	Nut, KEPS (AP)	2		PAOZZ
	H-6768	96906	Nut, KEPS (AP)	2		PAOZZ
8	10350-A-1032-2	06540	Handle	2		XB
	MS24693-C272	96906	Screw, Machine (AP)	4		PAOZZ
9	H408-1	83014	Catch, Clamping	4		PAOZZ
	MS51957-4	96906	Screw, Machine (AP)	8		PAOZZ
	MS35338-134	96906	Washer, Split (AP)	8		PAOZZ

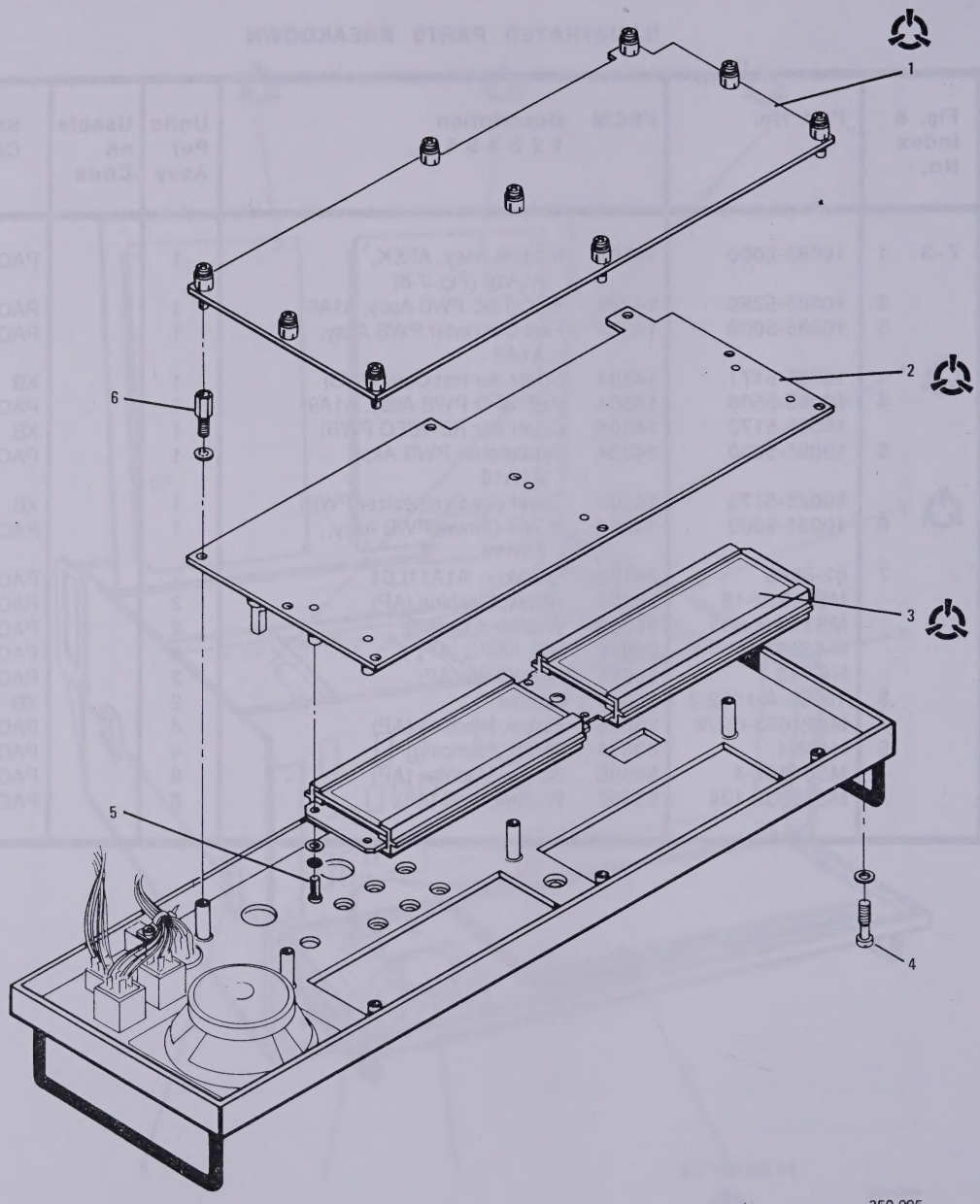


Figure 7-4. 100 Watt Transceiver, RT-1446/URC, Front Panel Assembly

ILLUSTRATED PARTS BREAKDOWN

Fig. & Index No.	Part No.	FSCM	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code	SMR Code
7- 4-	10085-2000	14304	Front Panel Assy, A1A11	1		PAODD
1	10088-6000	14304	. R/C Interface PWB Assy, A1A19*	1		PAODD
2	10085-2100	14304	. Front Panel PWB Assy, A1A11A1	1		PAODD
3	10085-2110	14304	. Display Assy, A1A11A2	1		PAOLD
4	10087-2012	14304	. Screw, Machine	4		PAOZZ
	10087-2011	14304	. Washer, Flat	4		PAOZZ
5	MS51957-14	96906	. Screw, Machine	6		PAOZZ
	MS35338-135	96906	. Washer, Split	6		PAOZZ
	MS15795-803	96906	. Washer, Flat	6		PAOZZ
6	9725-SS-0440-7	06540	. Spacer	9		PAOZZ
	MS35333-70	96906	. Washer, Lock	9		PAOZZ

*Not included with the Front Panel Assembly. Included with Remote Control Unit C-11329/URC.

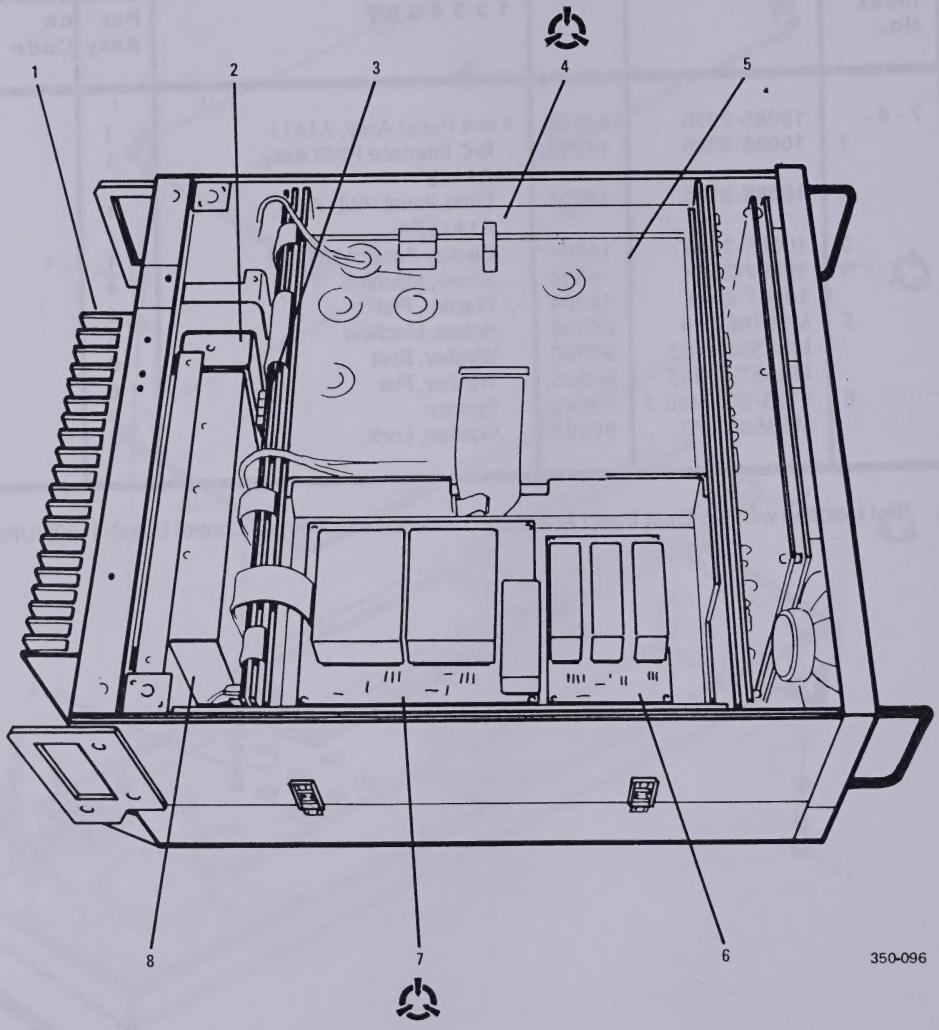
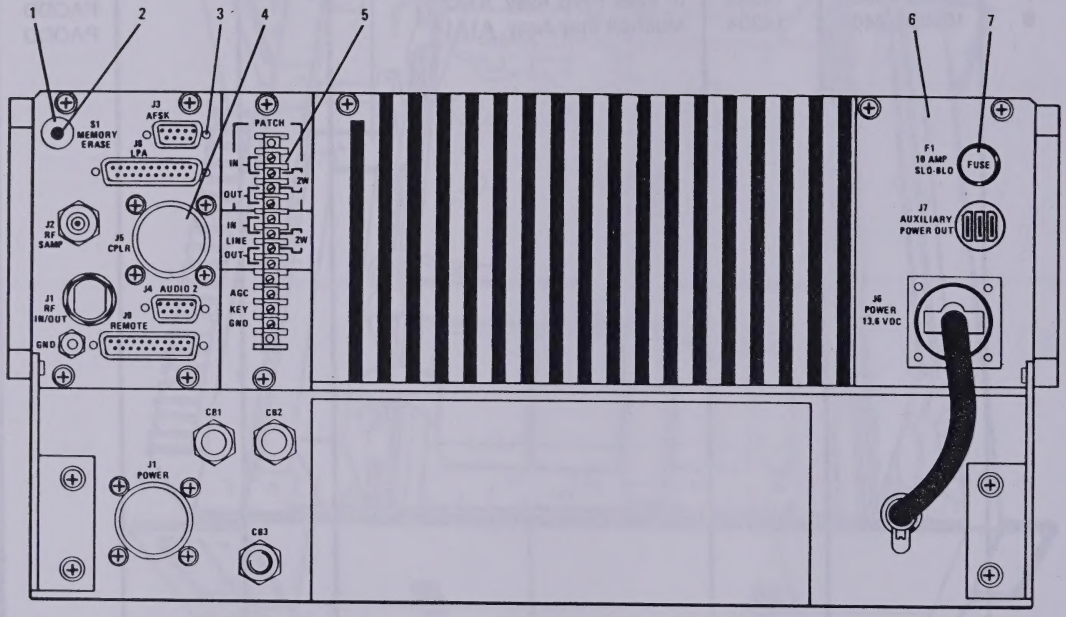


Figure 7-5. 100 Watt Transceiver, RT-1446/URC, Top Side View

ILLUSTRATED PARTS BREAKDOWN

Fig. & Index No.	Part no.	FSCM	Description 1 2 3 4 5 6 7	Units Per	Usable on Assy	SMR Code Code
7-5- 1	10085-8010	14304	100W PA, 12V, Assy, A1A4	1		PAOLD
2	10085-0610	14304	Oscillator Assy, RF, A1A8	1		PAOZZ
3	10085-4210	14304	Interconnect PWB Assy, A1A15	1		PADLD
4	10085-7000	14304	LPA/CPLR Intfc PWB Assy, A1A13	1		PAODD
5	10085-4000	14304	Low Pass Filter PWB Assy, A1A5	1		PAODD
	10085-5106	14304	Cover (for Low Pass Filter)	1		XB
6	10085-6000	14304	Module Assy, AFSK, A1A18 (fig. 7-8)	1		PAODD
7	10085-5300	14304	IF Filter PWB Assy, A1A2	1		PAODD
8	10085-1240	14304	Multivolt Sply Assy, A1A14	1		PAODD



350-097

Figure 7-6. 100 Watt Transceiver, RT-1446/URC, Rear View

ILLUSTRATED PARTS BREAKDOWN

Fig. & Index No.	Part no.	FSCM	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code	SMR Code
7-6- 1	G-12-A	95146	Cover, Switch	1		PAOZZ
2	3101-1261	28482	Switch, Push Button, A1S1	1		PAOZZ
3	205817-1	00779	Retainer	1		XB
4	10085-0550	14304	CPLR Conn PWB Assy, A1A17	1		PAOLD
5	10085-0570	14304	Audio Intfc PWB Assy, A1A16	1		PAODD
6	10085-0580	14304	Conn Plate Assy, A1A20	1		PAODD
7	FO2B32V10A	81349	Fuse, Slow-Blow, A1A20F1	1		PAOZZ

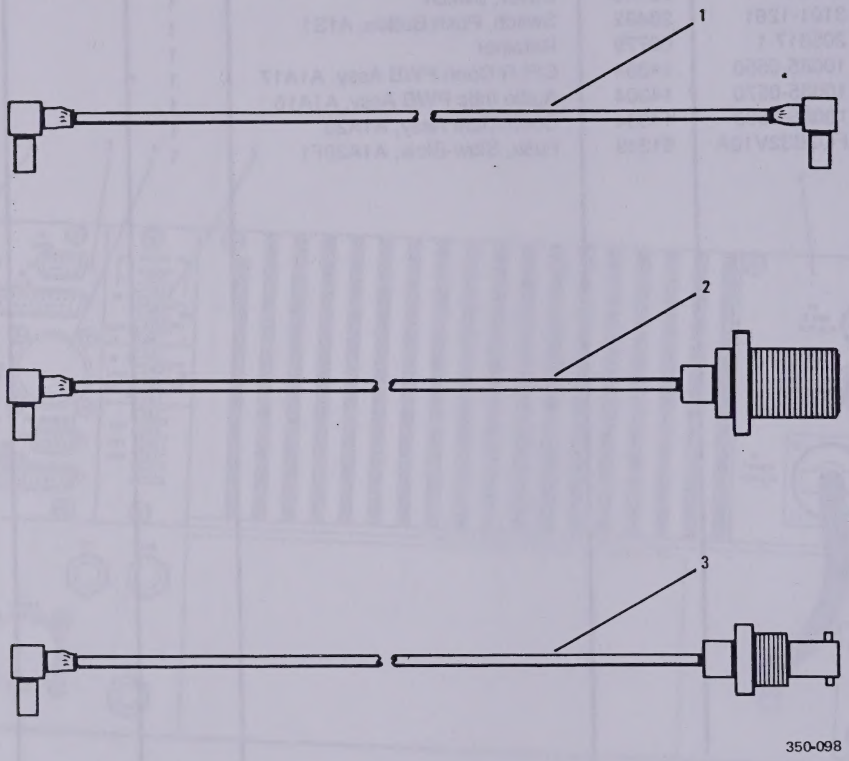
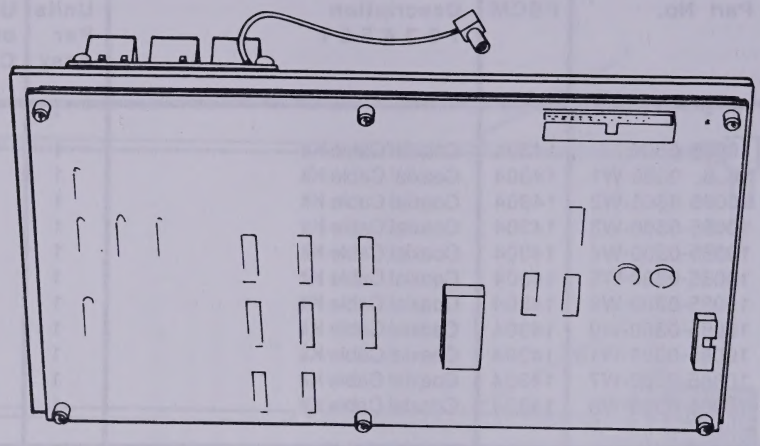


Figure 7-7. Coaxial Cable Kit

ILLUSTRATED PARTS BREAKDOWN

Fig. & Index No.	Part No.	FSCM	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code	SMR Code
7-7-	10085-0300	14304	Coaxial Cable Kit	1		PAOZZ
1	10085-0300-W1	14304	Coaxial Cable Kit	1		XB
	10085-0300-W2	14304	Coaxial Cable Kit	1		XB
	10085-0300-W3	14304	Coaxial Cable Kit	1		XB
	10085-0300-W4	14304	Coaxial Cable Kit	1		XB
	10085-0300-W5	14304	Coaxial Cable Kit	1		XB
	10085-0300-W6	14304	Coaxial Cable Kit	1		XB
	10085-0300-W9	14304	Coaxial Cable Kit	1		XB
	10085-0300-W13	14304	Coaxial Cable Kit	1		XB
2	10085-0300-W7	14304	Coaxial Cable Kit	1		XB
3	10085-0300-W8	14304	Coaxial Cable Kit	1		XB



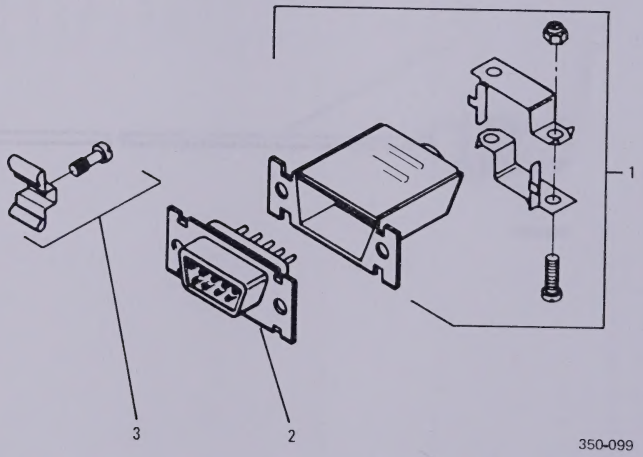
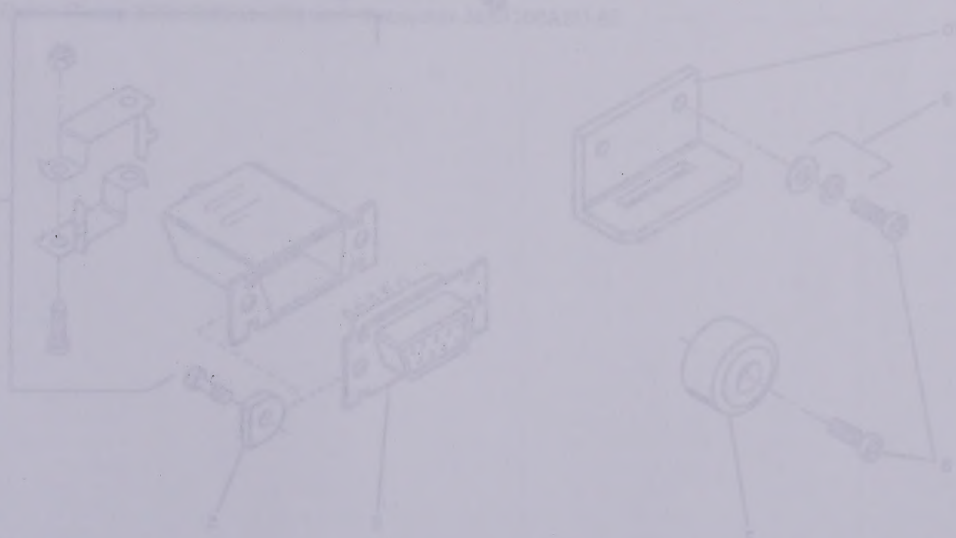


Figure 7-8. Module Assy, AFSK

ILLUSTRATED PARTS BREAKDOWN

Fig. & Index No.	Part No.	FSCM	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code	SMR Code
7-8-	10085-6000	14304	Module Assy, AFSK, A1A18	1		PAODD
1	DE24657	71468	. Hood	1		PAOZZ
2	DEM9P	71468	. Connector	1		PAOZZ
3	D20419-16	71468	. Fastener, Screw-Lock	2		PAOZZ



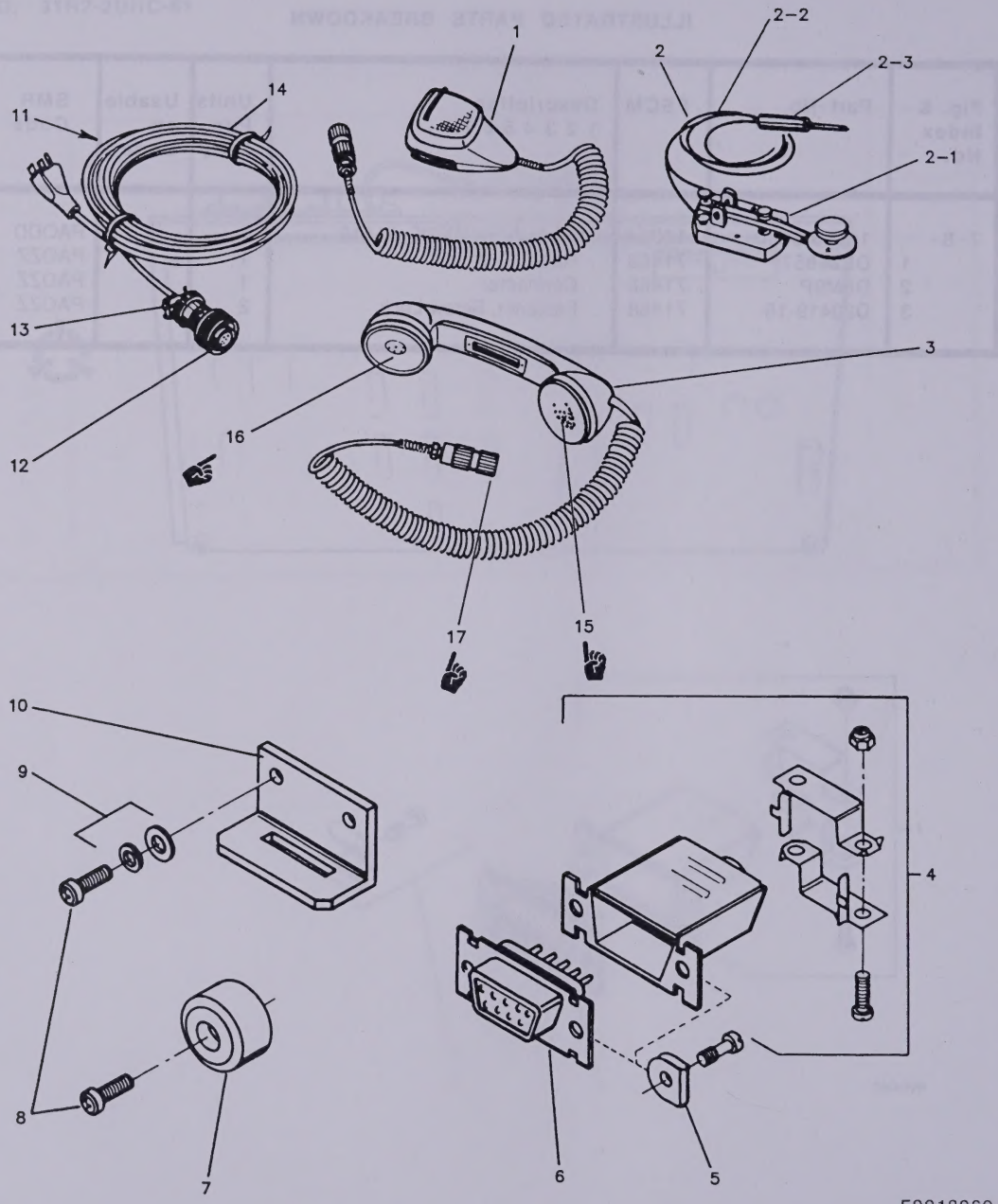


Figure 7-9. Installation Kit for the 100 Watt Transceiver

FIGURE & INDEX NUMBER	PART NUMBER	FSCM	1 2 3 4 5 6 7 DESCRIPTION	UNITS PER ASSY	USABLE ON CODE	SMR CODE
			ILLUSTRATED PARTS BREAKDOWN			
7-9-	10085-0060	14304	Installation Kit	1		XB
1-	10085-0068	14304	. Microphone	1		PAOZZ
2-	10085-0066	14304	. CW Key Assy	1		XB
-1	274-9000-00	13499	. Key, Telegraph	1		PAOZZ
-2	8761	70903	. Cable	1		PAOZZ
-3	M642/4-1	81349	. Plug, Telephone	1		PAOZZ
3-	10085-0067	14304	. Handset	1		XB
4-	DE24657	71468	. Hood	1		PAOZZ
5-	D-20419-16	94033	. Fastener, Screw, Lock	2		PAOZZ
6-	M24308/1-1	81349	. Connector, Rcpt. Elec	1		PAOZZ
7-	827S	70485	. Bumper, Rubber	4		PAOZZ
8-	MS51957-28	96906	. Screw, Machine	12		PAOZZ
9-	MS35338-136	96906	. Washer, Lock	8		PAOZZ
	MS15795-805	96096	. Washer, Flat	8		PAOZZ
10-	10087-3106	14304	. Bracket, Angle	4		XB
11-	10085-0065	14304	. Cable Assy*	1		XB
12-	MS3106A20-8S	96906	. Connector, Rcpt, Elec	1		PAOZZ
13-	MS85049/41-12A	81349	. Clamp, Cable	1		PAOZZ
14-	17517	70903	. Power Cable	1		PAOZZ
3-15	1938	97101	Microphone dynamic	1		PAOZZ
-16	2444V	64957	Ear phone	1		PAOZZ
-17	U-229/U	91662	Connector, Plug, Elec.	1		PAOZZ

*Includes Cable Clamp MS85049/41-12A and Connector MS3106A2O-8S

Fig. & Index No.	Part no.	FSCM	Description 1 2 3 4 5 6 7	Units Per Assy	Usable on Code	SMR Code
7-10-1	10085-0322	14304	Cable Assy: Front Panel XCVR Control-Exciter	1		PAOZZ
2	10085-0324	14304	Cable Assy: Exciter-Synthesizer Receiver-LPA/Coupler Int.-XCVR Control-Interconnect	1		PAOZZ
3	10085-0346	14304	Cable Assy: Aud 2 Connector-Audio Interface-Exciter-Interconnect	1		PAOZZ
4	10088-6007	14304	Cable Assy: Remote Control Connector-Remote Control Interface-Audio Interface	1		PAOZZ
5	10085-0329	14304	Cable Assy: Interconnect-Keyer/Converter	1		PAOZZ
6	10085-0330	14304	Cable Assy: AFSK Connector-Keyer/Converter	1		PAOZZ

Figure 7-10. Non-Pendant Cable List

REFERENCE DESIGNATOR INDEX

Reference Designator	Fig. & Index No.	Part Number	Reference Designator	Fig. & Index No.	Part Number
A1	7-1-1	10085-0100		7-3-1	
A1A1	7-1-10	10085-5400	A1A18	7-5-6	10085-6000
A1A2	7-5-7	10085-5300		7-8	
A1A3	7-3-3	10085-5000	A1A18W1	7-10-5	10085-0329
A1A4	7-5-1	10085-8010	A1A18W2	7-10-6	10085-0330
A1A5	7-5-5	10085-4000	A1A19	7-4-1	10088-6000
A1A6	7-3-2	10085-5250	A1A19W1	7-10-4	10088-6007
A1A7	7-1-3	10085-5200	A1A20	7-6-6	10085-0580
A1A8	7-5-2	10085-0610	A1A20F1	7-6-7	10018550-104
A1A9	7-3-4	10085-5500	A1W1-A1W9, A1W13	7-7	10085-0300
A1A10	7-3-5	10085-5600	A1W10	7-10-1	10085-0322
A1A11	7-4	10085-2000	A1W11	7-10-2	10085-0324
A1A11A1	7-4-2	10085-2100	A1W12	7-10-3	10085-0346
A1A11A2	7-4-3	10085-2110	A2	7-2	10085-0200
A1A11LS1	7-3-7	82-8666	A2A1	7-2-5	10085-0290
A1A11S1	7-1-5	7401T1ZGE	A2A2	7-2-10	10085-0260
A1A11KP1	7-1-9	10085-2007	A2A3	7-2-12	10085-0240
A1A12	7-3-6	10085-9000	A2B1	7-2-1	028868
A1A13	7-5-4	10085-7000	A2C1	7-2-4	C21-0006-663
A1A14	7-5-8	10085-1240	A2CB1, A2CB2	7-2-2	W58XB1A6A-6
A1A15	7-5-3	10085-4210	A2CB3	7-2-3	41-3-S14-LN2-50
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DE24657	7-8-1	2
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DEM9P	7-8-2	1
F4-30-SS	7-2-14	1
FO2B32V10A	7-6-7	1
G-12-A	7-6-1	1
H408-1	7-3-9	4
H-6768	7-3-7	2
H6769	7-3-7	2
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M642/4-1	7-9-2-3	1
MS15795-803	7-2-8	10
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MS15795-807	7-2-8	2
MS15795-805	7-9-9	8
MS15795-808	7-2-6	4
MS24693-C272	7-3-8	4
MS3106A20-8S	7-9-12	1
MS35333-70	7-4-6	9
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MS51957-16	7-2-8	2
MS51957-18	7-3-7	2
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MS51958-72	7-2-6	4
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10085-0010	7-1-1	1
10085-0060	7-9	1
10085-0065	7-9-11	1
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10085-0067	7-9-3	1
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10085-0257	7-2-8	1
10085-0260	7-2-10	1
10085-0263	7-2-11	1
10085-0273	7-2-8	1
10085-0278	7-2-6	2
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10085-0300-W3	7-7-1	1
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10085-0324	7-10-2	1
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10085-5172	7-3-4	1
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10085-9000	7-3-6	1
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1938	7-9-3-15	1
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